COMPREHENSIVE SERVICES

We offer competitive repair and calibration services, as well as easily accessible documentation and free downloadable resources.

SELL YOUR SURPLUS

We buy new, used, decommissioned, and surplus parts from every NI series. We work out the best solution to suit your individual needs.

Sell For Cash Get Credit Receive a Trade-In Deal

OBSOLETE NI HARDWARE IN STOCK & READY TO SHIP

We stock **New, New Surplus, Refurbished,** and **Reconditioned** NI Hardware.

APEX WAVES

Bridging the gap *between the manufacturer and your legacy test system.*

1-800-915-6216

www.apexwaves.com

sales@apexwaves.com

Request a Quote CLICK HERE *USB-4431*

NI Dynamic Signal Acquisition

NI Dynamic Signal Acquisition User Manual

Français Deutsch 日本語 한국어 简体中文

ni.com/manuals

November 2010
371235H-01

NATIONAL INSTRUMENTS

Worldwide Technical Support and Product Information

ni.com

National Instruments Corporate Headquarters

11500 North Mopac Expressway Austin, Texas 78759-3504 USA Tel: 512 683 0100

Worldwide Offices

Australia 1800 300 800, Austria 43 662 457990-0, Belgium 32 (0) 2 757 0020, Brazil 55 11 3262 3599, Canada 800 433 3488, China 86 21 5050 9800, Czech Republic 420 224 235 774, Denmark 45 45 76 26 00, Finland 358 (0) 9 725 72511, France 01 57 66 24 24, Germany 49 89 7413130, India 91 80 41190000, Israel 972 3 6393737, Italy 39 02 41309277, Japan 0120-527196, Korea 82 02 3451 3400, Lebanon 961 (0) 1 33 28 28, Malaysia 1800 887710, Mexico 01 800 010 0793, Netherlands 31 (0) 348 433 466, New Zealand 0800 553 322, Norway 47 (0) 66 90 76 60, Poland 48 22 328 90 10, Portugal 351 210 311 210, Russia 7 495 783 6851, Singapore 1800 226 5886, Slovenia 386 3 425 42 00, South Africa 27 0 11 805 8197, Spain 34 91 640 0085, Sweden 46 (0) 8 587 895 00, Switzerland 41 56 2005151, Taiwan 886 02 2377 2222, Thailand 662 278 6777, Turkey 90 212 279 3031, United Kingdom 44 (0) 1635 523545

For further support information, refer to the *Technical Support and Professional Services* appendix. To comment on National Instruments documentation, refer to the National Instruments Web site at ni.com/info and enter the Info Code feedback.

Important Information

Warranty

The NI USB-4431/4432, NI 4461/4462, NI 4472/4472B/4474, and NI 4492/4495/4496/4497/4498/4499 are warranted against defects in materials and workmanship for a period of one year from the date of shipment, as evidenced by receipts or other documentation. National Instruments will, at its option, repair or replace equipment that proves to be defective during the warranty period. This warranty includes parts and labor.

The media on which you receive National Instruments software are warranted not to fail to execute programming instructions, due to defects in materials and workmanship, for a period of 90 days from date of shipment, as evidenced by receipts or other documentation. National Instruments will, at its option, repair or replace software media that do not execute programming instructions if National Instruments receives notice of such defects during the warranty period. National Instruments does not warrant that the operation of the software shall be uninterrupted or error free.

A Return Material Authorization (RMA) number must be obtained from the factory and clearly marked on the outside of the package before any equipment will be accepted for warranty work. National Instruments will pay the shipping costs of returning to the owner parts which are covered by warranty.

National Instruments believes that the information in this document is accurate. The document has been carefully reviewed for technical accuracy. In the event that technical or typographical errors exist, National Instruments reserves the right to make changes to subsequent editions of this document without prior notice to holders of this edition. The reader should consult National Instruments if errors are suspected. In no event shall National Instruments be liable for any damages arising out of or related to this document or the information contained in it.

EXCEPT AS SPECIFIED HEREIN, NATIONAL INSTRUMENTS MAKES NO WARRANTIES, EXPRESS OR IMPLIED, AND SPECIFICALLY DISCLAIMS ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. CUSTOMER'S RIGHT TO RECOVER DAMAGES CAUSED BY FAULT OR NEGLIGENCE ON THE PART OF NATIONAL INSTRUMENTS SHALL BE LIMITED TO THE AMOUNT THERETOFORE PAID BY THE CUSTOMER. NATIONAL INSTRUMENTS WILL NOT BE LIABLE FOR DAMAGES RESULTING FROM LOSS OF DATA, PROFITS, USE OF PRODUCTS, OR INCIDENTAL OR CONSEQUENTIAL DAMAGES, EVEN IF ADVISED OF THE POSSIBILITY THEREOF. This limitation of the liability of National Instruments will apply regardless of the form of action, whether in contract or tort, including negligence. Any action against National Instruments must be brought within one year after the cause of action accrues. National Instruments shall not be liable for any delay in performance due to causes beyond its reasonable control. The warranty provided herein does not cover damages, defects, malfunctions, or service failures caused by owner's failure to follow the National Instruments installation, operation, or maintenance instructions; owner's modification of the product; owner's abuse, misuse, or negligent acts; and power failure or surges, fire, flood, accident, actions of third parties, or other events outside reasonable control.

Copyright

Trademarks

CVI, LabVIEW, National Instruments, NI, ni.com, the National Instruments corporate logo, and the Eagle logo are trademarks of National Instruments Corporation. Refer to the *Trademark Information* at `ni.com/trademarks` for other National Instruments trademarks.

The mark LabWindows is used under a license from Microsoft Corporation. Windows is a registered trademark of Microsoft Corporation in the United States and other countries. Other product and company names mentioned herein are trademarks or trade names of their respective companies.

Members of the National Instruments Alliance Partner Program are business entities independent from National Instruments and have no agency, partnership, or joint-venture relationship with National Instruments.

Patents

For patents covering National Instruments products/technology, refer to the appropriate location: **Help»Patents** in your software, the `patents.txt` file on your media, or the *National Instruments Patent Notice* at `ni.com/patents`.

WARNING REGARDING USE OF NATIONAL INSTRUMENTS PRODUCTS

(1) NATIONAL INSTRUMENTS PRODUCTS ARE NOT DESIGNED WITH COMPONENTS AND TESTING FOR A LEVEL OF RELIABILITY SUITABLE FOR USE IN OR IN CONNECTION WITH SURGICAL IMPLANTS OR AS CRITICAL COMPONENTS IN ANY LIFE SUPPORT SYSTEMS WHOSE FAILURE TO PERFORM CAN REASONABLY BE EXPECTED TO CAUSE SIGNIFICANT INJURY TO A HUMAN.

(2) IN ANY APPLICATION, INCLUDING THE ABOVE, RELIABILITY OF OPERATION OF THE SOFTWARE PRODUCTS CAN BE IMPAIRED BY ADVERSE FACTORS, INCLUDING BUT NOT LIMITED TO FLUCTUATIONS IN ELECTRICAL POWER SUPPLY, COMPUTER HARDWARE MALFUNCTIONS, COMPUTER OPERATING SYSTEM SOFTWARE FITNESS, FITNESS OF COMPILERS AND DEVELOPMENT SOFTWARE USED TO DEVELOP AN APPLICATION, INSTALLATION ERRORS, SOFTWARE AND HARDWARE COMPATIBILITY PROBLEMS, MALFUNCTIONS OR FAILURES OF ELECTRONIC MONITORING OR CONTROL DEVICES, TRANSIENT FAILURES OF ELECTRONIC SYSTEMS (HARDWARE AND/OR SOFTWARE), UNANTICIPATED USES OR MISUSES, OR ERRORS ON THE PART OF THE USER OR APPLICATIONS DESIGNER (ADVERSE FACTORS SUCH AS THESE ARE HEREAFTER COLLECTIVELY TERMED "SYSTEM FAILURES"). ANY APPLICATION WHERE A SYSTEM FAILURE WOULD CREATE A RISK OF HARM TO PROPERTY OR PERSONS (INCLUDING THE RISK OF BODILY INJURY AND DEATH) SHOULD NOT BE RELIANT SOLELY UPON ONE FORM OF ELECTRONIC SYSTEM DUE TO THE RISK OF SYSTEM FAILURE. TO AVOID DAMAGE, INJURY, OR DEATH, THE USER OR APPLICATION DESIGNER MUST TAKE REASONABLY PRUDENT STEPS TO PROTECT AGAINST SYSTEM FAILURES, INCLUDING BUT NOT LIMITED TO BACK-UP OR SHUT DOWN MECHANISMS. BECAUSE EACH END-USER SYSTEM IS CUSTOMIZED AND DIFFERS FROM NATIONAL INSTRUMENTS' TESTING PLATFORMS AND BECAUSE A USER OR APPLICATION DESIGNER MAY USE NATIONAL INSTRUMENTS PRODUCTS IN COMBINATION WITH OTHER PRODUCTS IN A MANNER NOT EVALUATED OR CONTEMPLATED BY NATIONAL INSTRUMENTS, THE USER OR APPLICATION DESIGNER IS ULTIMATELY RESPONSIBLE FOR VERIFYING AND VALIDATING THE SUITABILITY OF NATIONAL INSTRUMENTS PRODUCTS WHENEVER NATIONAL INSTRUMENTS PRODUCTS ARE INCORPORATED IN A SYSTEM OR APPLICATION, INCLUDING, WITHOUT LIMITATION, THE APPROPRIATE DESIGN, PROCESS AND SAFETY LEVEL OF SUCH SYSTEM OR APPLICATION.

Compliance

Electromagnetic Compatibility Guidelines

This product was tested and complies with the regulatory requirements and limits for electromagnetic compatibility (EMC) as stated in the product specifications. These requirements and limits are designed to provide reasonable protection against harmful interference when the product is operated in its intended operational electromagnetic environment.

This product is intended for use in industrial locations. There is no guarantee that harmful interference will not occur in a particular installation, when the product is connected to a test object, or if the product is used in residential areas. To minimize the potential for the product to cause interference to radio and television reception or to experience unacceptable performance degradation, install and use this product in strict accordance with the instructions in the product documentation.

Furthermore, any changes or modifications to the product not expressly approved by National Instruments could void your authority to operate it under your local regulatory rules.

Caution To ensure the specified EMC performance, operate this product only with shielded cables and accessories.

Caution This product may become more sensitive to electromagnetic disturbances in the operational environment when test leads are attached or when connected to a test object.

Caution Emissions that exceed the regulatory requirements may occur when this product is connected to a test object.

Contents

Chapter 1
Getting Started

Chapter 2
Dynamic Signal Acquisition Device Concepts

Chapter 3
Developing Your Dynamic Signal Acquisition Application

Appendix A
Device-Specific Information

Appendix B
Technical Support and Professional Services

Figures

Tables

1

Getting Started

This manual contains information about using National Instruments Dynamic Signal Acquisition (DSA) devices. These devices have 24-bit resolution and support sample rates of up to 204.8 kS/s. With excellent dynamic range, noise and distortion performance, and simultaneous sampling and synchronization capabilities, the DSA devices are well suited for many applications including, but not limited to:

- Audio testing
- Acoustic measurements
- Environmental noise testing
- Vibration analysis
- Noise, vibration, and harshness measurements
- Machine condition monitoring
- Rotating machinery evaluation

Installing the Software

Note Before installing the DSA device, you must install the software you plan to use with the device.

NI-DAQmx

Software support for the NI Dynamic Signal Acquisition products is provided by NI-DAQmx. The *DAQ Getting Started* guides, which you can download at `ni.com/manuals`, offer step-by-step NI-DAQmx instructions for installing software and hardware, configuring channels and tasks, and getting started developing an application. For detailed NI software version support, refer to the NI-DAQmx readme.

Other Software

If you are using other software, refer to the installation instructions that accompany your software.

Example Programs

The NI-DAQmx media contains example programs that you can use to get started programming with the NI Dynamic Signal Acquisition devices. Refer to the *DAQ Getting Started* guide that shipped with your device, and is also accessible from **Start»All Programs»National Instruments»NI-DAQ**, for more information.

Installing the Hardware

The *DAQ Getting Started* guides contains general information about how to install DSA devices, accessories, and cables.

Device Pinouts

Refer to the *NI-DAQmx Help* for DSA device pinout information. Select **Start»All Programs»National Instruments»NI-DAQ»NI-DAQmx Help**.

Information Resources

Refer to `ni.com/manuals` for the most recent documentation.

The following documentation might be useful when using NI Dynamic Signal Acquisition devices:

- The *NI USB-443x Specifications* contains all specifications for the NI USB-4431 and NI USB-4432 devices.
- The *NI 446x Specifications* contains all specifications for the NI PCI-4461, NI PXI-4461, NI PCI-4462, and NI PXI-4462 devices.
- The *NI 447x Specifications* contains all specifications for the NI PCI-4472, NI PXI-4472, NI PCI-4474, NI PCI-4472B, and NI PXI-4472B devices.
- The *NI 449x Specifications* contains all specifications for the NI PXIe-4492, NI PXI-4495, NI PXI/PXIe-4496, NI PXIe-4497, NI PXI/PXIe-4498, and NI PXIe-4499 devices.

Measurement System Overview

A measurement system can consist of several components. Refer to the *DAQ Getting Started* guides for a measurement system overview of measurement applications.

Sensors and Transducers

A sensor or transducer is a device that outputs an electrical signal in response to a measured physical phenomenon such as pressure or temperature. The most common sensors for use with DSA devices include microphones for measuring sound pressure and accelerometers for measuring linear acceleration or vibration.

Refer to Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about typical DSA device measurements. You also can refer to the *NI-DAQmx Help* or the *LabVIEW Help* for more information about microphones, accelerometers, eddy current proximity probe sensors, or piezoelectric force sensors.

2

Dynamic Signal Acquisition Device Concepts

This chapter contains information about Dynamic Signal Acquisition (DSA) device concepts, including Nyquist frequency and bandwidth, noise, analog input and output, timing and triggering, and synchronization.

Nyquist Frequency and Nyquist Bandwidth

Any sampling system, such as an *ADC*, is limited in the bandwidth of the signals it can measure. Specifically, a sampling rate of f_s can represent only signals with frequencies lower than $f_s/2$. This maximum frequency is known as the *Nyquist frequency.* The bandwidth from 0 Hz to the Nyquist frequency is the *Nyquist bandwidth*.

Noise

Caution Electromagnetic interference can adversely affect the measurement accuracy of the DSA products described in this document. The inputs and outputs of these products are not connected to chassis ground for functional reasons. Therefore, the outer conductor of any connected coaxial cable is not connected to chassis ground and the outer conductor will not act as a shield for unwanted noise. The shield can act as an antenna to transmit noise into the environment or receive noise from the environment that could affect measurement accuracy. To ensure proper shielding effectiveness of connected coaxial cables, the outer conductor must be directly connected to chassis or earth ground at the load end of the cable. In addition, snap-on ferrite beads or other remedial measures may be required to prevent unwanted emissions or immunity. Refer to the specifications of your product for more information about EMC performance.

DSA devices typically have a dynamic range of more than 110 dB. Several factors can degrade the noise performance of input channels, such as noise picked up from nearby electronic devices. DSA devices work best when kept as far away as possible from other plug-in devices, power supplies, disk drives, and computer monitors. Cabling is also critical. Use well-shielded coaxial or floating cables for all connections. Route the cables away from sources of interference such as computer monitors, switching power supplies, and fluorescent lights. Physical motion or deformation can induce noise on sensitive analog cables. Use a

transducer with a low output impedance to minimize system susceptibility to external noise sources and crosstalk.

You can reduce the effects of noise on your measurements by carefully choosing the sample rate to maximize the effectiveness of the anti-alias filtering. Computer monitor noise, for example, typically occurs at frequencies between 15 kHz and 65 kHz. If the signal of interest is restricted to below 10 kHz, for example, the anti-alias filters reject the monitor noise outside the frequency band of interest, and a sampling rate of at least 21.6 kS/s guarantees that any signal components in the 10 kHz bandwidth of interest are acquired without aliasing and without being attenuated by the digital filter. Refer to the *Analog Input Filters* section of this chapter for more information about anti-alias filtering.

When possible, use the differential configuration to minimize the effect of any noise produced by ground currents in the chassis and common-mode noise. If you have particularly noisy AC power, consider external filtering, such as a line conditioner or an uninterruptible power supply.

Analog Input

Analog Input Channel Configurations

The NI 446*x* supports two terminal configurations for analog input: *differential* and *pseudodifferential*. The NI USB-443*x*, NI 447*x* and NI 449*x* support only the pseudodifferential channel configuration. The term pseudodifferential refers to the 50 Ω or 1 kΩ resistance between the outer connector shell and chassis ground.

Note Attach PXI/PXIe and PCI devices to the chassis with screws to provide a reliable ground connection. If you use a PXI/PXIe device, tighten the screws at the top and bottom of the front face of the device. If you use a PCI device, keep the screw that held the PCI slot cover to the computer chassis. Reinsert this screw to securely attach the device. For USB-443*x* devices, connect the ground terminal on the back of the USB case to the chassis of the host PC.

Choosing Channel Configurations

If the signal source is floating, use the pseudodifferential configuration. The pseudodifferential configuration provides a ground reference between the floating source and the DSA device by connecting either a 50 Ω or 1 kΩ resistor (depending on the DSA device) from the negative input to ground. Without this, the floating source can drift outside of the common-mode range of the DSA device being used.

If the signal source is grounded or ground referenced, both the pseudodifferential and differential input configurations are acceptable. However, the differential input configuration is preferred, since using the pseudodifferential input configuration on a grounded signal

source creates more than one ground-reference point. This condition may allow ground loop currents, which can introduce errors or noise into the measurement. The 50 Ω or 1 kΩ resistor between the negative input and ground is usually sufficient to reduce these errors to negligible levels, but results can vary depending on your system setup.

Configure the channels based on the signal source reference or DUT configuration. Refer to Table 2-1 to determine how to configure the channel.

Table 2-1. Analog Input

Source Reference	Channel Configuration
Floating	Pseudodifferential
Grounded	Differential or pseudodifferential

The NI 446*x* is automatically configured for differential mode when powered on.

Input Coupling

You can configure the NI USB-443*x*, NI 446*x*, NI 447*x*, and a subset of the NI 449*x* devices for either AC or DC coupling with the AI.Coupling property. If you select DC coupling, any DC offset present in the source signal is passed to the ADC. The DC-coupling configuration is usually best if the signal source has only small amounts of offset voltage or if the DC content of the acquired signal is important. If the source has a significant amount of unwanted offset, select AC coupling to take full advantage of the input dynamic range.

Note The NI 4496 and NI 4498 provide AC coupling only. The NI 4495 provides DC coupling only. The NI 4492, NI 4497, and NI 4499 provide selectable AC/DC coupling.

Selecting AC coupling enables a highpass resistor-capacitor (RC) filter into the signal conditioning path. The filter time constant is 47 ms for the NI 446*x*, NI 4472, and NI PCI-4474. The highpass RC filter settles to 0.5% accuracy in 0.25 s in response to a step input. It takes 0.782 s to settle to 24-bit accuracy in response to a step input. The settling time is somewhat dependent on the DUT impedance as well.

The NI 4472B and NI 449*x* have a larger time constant (330 ms). It takes 5.5 s to settle to 24-bit accuracy in response to a step input.

Note NI-DAQmx does not compensate for the settling time introduced by the RC filter when switching from DC to AC coupling. To compensate for the filter settling time, you can discard the samples taken during the settling time or force a delay before you restart the measurement. You must force the delay after the AI task is committed, but before the task starts.

Using AC coupling results in an attenuation of the low-frequency response of the AI circuitry. Refer to the *NI USB-443x Specifications, NI 446x Specifications*, *NI 447x Specifications*, and *NI 449x Specifications* for information about the cut-off frequency for each device.

TEDS (Transducer Electronic Data Sheet)

TEDS-capable sensors carry a built-in, self-identification EEPROM that stores a table of parameters and sensor information. TEDS sensors have two modes of operation: an analog mode that allows the sensors to operate as transducers measuring physical phenomena, and a digital mode that allows you to write and read information to and from the TEDS. The NI USB-443*x*, NI PCI-4461, NI PXI-4461 (Revision M or later), NI 4462, and NI 449*x* support modes for Class I TEDS sensors without any additional hardware[1]. The NI 447*x* devices require an accessory, such as the BNC-2096, to allow digital communication with the EEPROM on Class I TEDS sensors.

TEDS contains information about the sensor such as calibration, sensitivity, and manufacturer information. This information is accessible in Measurement & Automation Explorer (MAX), VIs in LabVIEW, or by calling the equivalent function calls in a text-based ADE.

Refer to the following installed help files for more information about TEDS:

- *Measurement & Automation Explorer Help for NI-DAQmx*—Contains information about configuring and testing data acquisition (DAQ) devices, RT Series DAQ devices, SCXI devices, SCC devices, TEDS carriers, and RTSI cables using MAX for NI-DAQmx, and special considerations for operating systems. Select **Help»Help Topics»NI-DAQmx» MAX Help for NI-DAQmx** in MAX.
- *NI-DAQmx Help*—Contains general information about measurement concepts, key NI-DAQmx concepts, and common applications that are applicable to all programming environments. Select **Start»All Programs»National Instruments»NI-DAQ» NI-DAQmx Help**.
- *LabVIEW Help*—Contains information about LabVIEW programming concepts, step-by-step instructions for using LabVIEW, and reference information about LabVIEW VIs, functions, palettes, menus, and tools.

You also can refer to the following pages on `ni.com` for more information. Go to `ni.com/info` and enter the Info Code.

- *Smart Sensors*—Info Code `rdsenr`
- *What Are Plug & Play Sensors?*—Info Code `rdpnpy`
- *IEEE 1451.4 Sensor Templates Overview*—Info Code `rdted6`

[1] The NI 4495 does not support TEDS.

IEPE

If you attach an *IEPE* accelerometer or microphone that requires excitation to an AI channel of the DSA device, you must enable the IEPE excitation circuitry for that channel to generate the required excitation current. You can independently configure IEPE signal conditioning on a per channel basis on all DSA devices.

A DC voltage offset is generated equal to the product of the excitation current and sensor impedance when IEPE signal conditioning is enabled. To remove the unwanted offset, enable AC coupling. DC coupling can be used with IEPE excitation enabled without a loss of signal integrity only if the offset plus the peak of the AC signal of interest does not exceed the voltage range of the channel.

Common IEPE excitation values are 2.1 mA, 4 mA, and 10 mA. Refer to the *NI USB-443x Specifications, NI 446x Specifications*, *NI 447x Specifications*, and *NI 449x Specifications* for a list of supported IEPE current values for each device.

Note You must set the NI 446*x* inputs to pseudodifferential mode when IEPE is activated.

Overload Detection

When the signal voltage exceeds the input range, distortion caused by a clipped or overranged waveform can occur. The NI 446*x* devices include overload detection in both the analog domain (predigitization) and digital domain (postdigitization). The NI USB-443*x*, NI 447*x*, and NI 449*x* devices support digital domain overload detection. Use the OverloadedChansExist and OverloadedChans properties to access the overload detection feature.

An analog overrange can occur independently from a digital overrange, and vice versa. For example, an IEPE accelerometer might have a resonant frequency that, when stimulated, can produce an overrange in the analog signal. However, because the ADC delta-sigma technology uses very sharp anti-aliasing filters, the overrange is not passed into the digitized signal.

Conversely, a sharp transient on the analog side might not overrange, but the step response of the delta-sigma anti-aliasing filters might produce clipping in the digital data. The NI 446*x* analog overload detection circuitry detects a clipped or overloaded condition. You can programmatically poll the overload detection circuitry on a per channel basis to monitor for an overload condition. If an overload is detected, consider any data acquired at that time corrupt.

DSA devices perform digital overload detection as a percentage of the range. The overload detection occurs before the device applies gain and offset corrections. Detecting the overload before the gain and offset corrections catches an overflow condition in the delta-sigma modulator or ADC filter.

For instance, on NI 446*x* DSA devices, the analog overload point for the 0 dB gain range is approximately 10.7 V_{pk}. This is the voltage at which the front-end circuitry begins showing signs of saturation. Figure 2-1 shows harmonic aliases caused by clipping with a 1.0 kHz sine wave at 10.8 V_{pk}, versus the same signal at 8.9 V_{pk}, which shows no clipping, on an NI 446*x* device. NI USB-443*x*, NI 447*x,* and NI 449*x* devices display similar behavior.

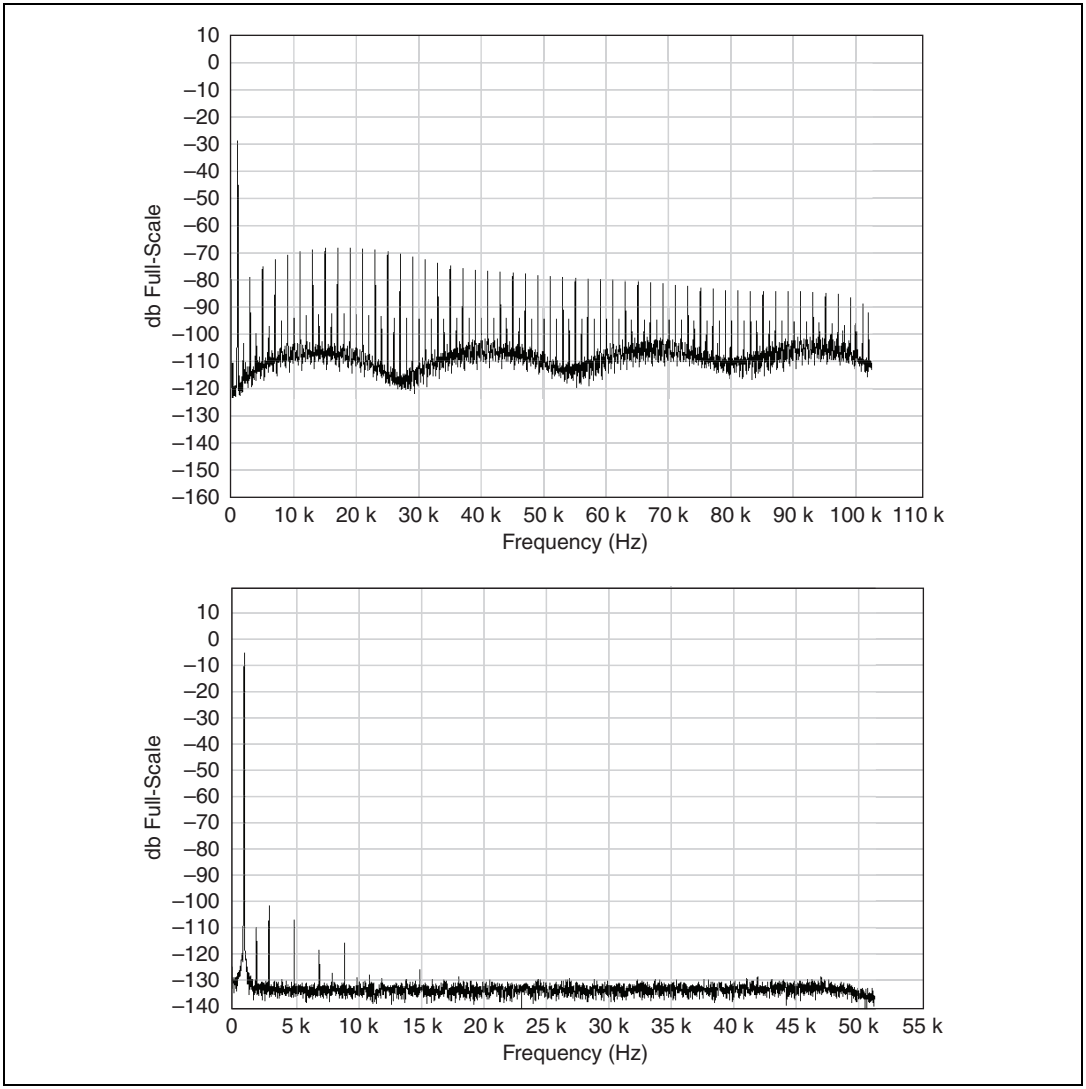

Figure 2-1. NI 446*x* Harmonic Aliases

Caution For NI 446*x* devices, overload detection is not supported for the ±42.4 V_{pk} input range setting. This setting attenuates the signal by a factor of 10. This attenuation factor implies that the ADC reaches the analog saturation point at 115 V_{pk}. This level is greater than what the ±42.4 V_{pk} range can safely support. You risk damaging the input circuitry when measuring voltages capable of producing an overload condition when you use the ±42.4 V_{pk} range (–20 dB gain) setting.

ADC

Each ADC in a DSA device uses a conversion method known as delta-sigma modulation. If the desired data rate is 51.2 kS/s, each ADC actually samples its input signal at 6.5536 MS/s, 128 times the data rate (or depending on the device and mode, it could be 256 times the data rate or another power of 2 multiple of the data rate), producing 1-bit samples that are sent to a digital filter. This filter rejects signal components greater than the Nyquist frequency of 25.6 kHz. The 1-bit, 6.5536 MS/s data stream from the ADC contains all of the information necessary to produce 24-bit samples at 51.2 kS/s. The delta-sigma ADC achieves this conversion from high speed to high resolution with a technique called noise shaping. The ADC adds random noise to the signal so that the resulting quantization noise, although large, is restricted to frequencies above the Nyquist frequency, 25.6 kHz in this case. This noise is not correlated with the input signal and is almost completely rejected by the digital filter.

The resulting output of the filter is a band-limited signal with a large dynamic range. One of the advantages of a delta-sigma ADC is that it uses a 1-bit DAC as an internal reference. As a result, the delta-sigma ADC is free from the differential nonlinearity (DNL) and associated noise inherent in high-resolution ADCs using other conversion techniques.

Analog Input Filters

Anti-Alias Filters

A digitizer or ADC might sample signals containing frequency components above the Nyquist limit. The undesirable effect of the digitizer modulating out-of-band components into the Nyquist bandwidth is aliasing. The greatest danger of aliasing is that you cannot determine whether aliasing occurred by looking at the ADC output. If an input signal contains several frequency components or harmonics, some of these components might be represented correctly while others contain aliased artifacts.

Lowpass filtering to eliminate components above the Nyquist frequency either before or during the digitization process can guarantee that the digitized data set is free of aliased components. DSA devices employ both digital and analog lowpass filters to achieve this protection.

The delta-sigma ADCs on DSA devices include an oversampled architecture and sharp digital filters with cut-off frequencies that track the sampling rate. Thus, the filter automatically adjusts to follow the Nyquist frequency. Although the digital filter eliminates almost all

out-of-band components, it is still susceptible to aliases from certain narrow frequency bands, defined by the following rules:

- When you select a sample rate greater than 102.4 kS/s and less than or equal to 204.8 kS/s, the susceptible areas are centered around 32, 64, 96, and other multiples of 32 f_s (NI 446*x* and NI 449*x* only, because only the NI 446*x* and NI 449*x* devices support sample rates higher than 102.4 kS/s).
- When you select a sample rate greater than 51.2 kS/s and less than or equal to 102.4 kS/s, the susceptible areas are centered around 64, 128, 192, and other multiples of 64 f_s.
- When you select a sample rate greater than or equal to the minimum rate for the specific DSA device and less than or equal to 51.2 kS/s, the susceptible areas are centered around 128, 256, 384 and other multiples of 128 f_s.

Note On the NI USB-443*x* the susceptible areas are at multiples of 64 f_s regardless of the sample rate.

The susceptible frequency band is always one f_s wide. For example, if f_s = 10,000 S/s, the digital filter can admit aliases from analog components between 1.275 MHz and 1.285 MHz.

In addition to the ADC built-in digital filtering, DSA devices feature a fixed-frequency analog filter. The analog filter removes high-frequency components in the analog signal path before they reach the ADC. This filtering addresses the possibility of high-frequency aliasing from the narrow bands that are not covered by the digital filter. Each input channel on a DSA device is equipped with a multiple pole lowpass analog filter.

While the frequency response of the digital filter directly scales with the sample rate, the analog filter –3 dB point is fixed. The analog filter response produces good high-frequency alias rejection while maintaining a flat in-band frequency response. Because the analog filters are not high-order systems, the filter roll-off is not extremely sharp. The filter provides effective alias rejection at higher sampling rates, where only very high frequencies in the previously mentioned susceptible areas can pass through the digital filter. Some DSA devices support enhanced low-frequency alias rejection. The NI USB-443*x*, NI 446*x*, NI 447*x*, and NI 449*x* devices have different filter response curves that are available in Appendix A, *Device-Specific Information*.

Low-Frequency Alias Rejection

At very low sample rates, between the minimum rate for the specific DSA device and 25.6 kS/s, the anti-aliasing filters of DSA device AI channels might not completely reject all out-of-band signals. The internal digital filter of the delta-sigma ADC cannot suppress signals with frequencies near the multiples of the oversample rate (sample rate multiplied by oversample factor). DSA devices also employ fixed cutoff analog lowpass anti-aliasing filters. At low sample rates, some multiples of the oversample rate can fall below the analog anti-aliasing filter cut-off frequency.

For example, for a device using ADCs with an oversample factor of 128 f_s and sampling at a rate of 1 kS/s, the oversample rate is 128 kHz. Some multiples of that oversample rate fall below the cut-off frequency of the analog anti-aliasing filter. If the signal contains energy near these frequencies, aliasing can result.

You can minimize aliasing by raising the sample rate so that the first 128 f_s multiple falls above the cut-off frequency of the analog anti-aliasing filter. For example, a sample rate of 25.6 kS/s is not subject to substantial aliasing because the first 128 f_s multiple, 3.2 MHz, is well above the analog anti-aliasing filter cut-off frequency. You can also enable low-frequency alias rejection with the AI.EnhancedAliasRejectionEnable property. This property causes the DSA device to automatically oversample for sample rates between 1 kS/s and 25.6 kS/s. The resulting oversampled rate always falls in the 25.6 kS/s to 51.2 kS/s range. The data stream is then decimated down by the same multiple to produce samples at the specified sample rate. Low-frequency alias rejection improves alias rejection near multiples of the oversample rate. This comes at the expense of alias rejection at other frequencies. For example, when sampling at 1 kS/s on the NI 446*x*, a 2 kHz tone is not close to a multiple of the oversample rate. The tone is attenuated by more than 120 dB. With low-frequency alias rejection enabled, the tone is only attenuated by 104 dB.

Table 2-2 lists the decimation factors for given sample rates. Refer to the *NI-DAQmx Help* or the *LabVIEW Help* for more information about the AI.EnhancedAliasRejectionEnable property.

Table 2-2. Decimation Factors for Given Sample Rates

Sample Rate	Decimation Factor
100 S/s ≤ f_s ≤ 200 S/s	256*
200 S/s < f_s ≤ 400 S/s	128*
400 S/s < f_s ≤ 800 S/s	64*
800 S/s < f_s ≤ 1.6 kS/s	32
1.6 kS/s < f_s ≤ 3.2 kS/s	16
3.2 kS/s < f_s ≤ 6.4 kS/s	8
6.4 kS/s < f_s ≤ 12.8 kS/s	4
12.8 kS/s < f_s ≤ 25.6 kS/s	2
* These decimation factors apply only to NI 449*x* devices.	

Not all DSA devices support low-frequency alias rejection. The following list provides more information about devices that support low-frequency alias rejection:

- NI 446*x* devices
- NI PXI-447*x* devices revision H and later
- NI PCI-447*x* devices revision F and later
- NI 449*x* devices

Note The AI.EnhancedAliasRejectionEnable property is enabled by default for NI 446*x* and disabled for NI 447*x* and NI 449*x* (for rates above 1 kS/s) devices.

Filter Delay

The filter delay is the time required for data to propagate through a converter. All DSA device channels have filter delays due to the presence of filter circuitry on both input and output channels. To understand how filter delay can affect your measurement, consider an ADC digital filter with a delay of 63 sample clock samples. At a 10 kS/s sample rate the signal experiences a delay equal to 6.3 ms.

The filter delay is an important factor for stimulus-response measurements, control applications, or any application where loop time is critical. Use the fastest allowable sample rate to minimize the effects of filter delay.

The input filter delay also makes an external digital trigger appear to occur earlier than expected. When acquiring from an ADC with a filter delay of 63 samples, and using a digital trigger to begin the acquisition, the first 63 samples of acquired data will have occurred before the digital trigger.

The NI 449*x* products support the AI.RemoveFilterDelay property. When enabled, the acquired data is automatically adjusted such that the first acquired sample is in line with the digital trigger. For more information, refer to the *Filter Delay Removal* section of this chapter.

Refer to the *NI USB-443x Specifications, NI 446x Specifications*, *NI 447x Specifications*, and *NI 449x Specifications* for information about filter delay for each device.

FIFO and PCI Data Transfer

DSA device input channels share a FIFO buffer, and the output channels share a separate FIFO buffer. The *NI USB-443x Specifications, NI 446x Specifications*, *NI 447x Specifications*, and *NI 449x Specifications* contain information about the buffer sample depth.

The devices have a flexible data transfer request condition. You can program the device to request DMA transfers according to a programmable FIFO condition. Refer to the *NI-DAQmx Help* or the *LabVIEW Help* for information about conditions available for specific devices.

Note USB devices do *not* allow setting the transfer request condition.

Analog Output (NI USB-4431 and NI 4461 Only)

Output Distortion

You can minimize output distortion by connecting the outputs to external devices with a high input impedance. Each output channel of the NI 4461 is rated to drive a minimal load of 600 Ω. Each output channel of the NI USB-4431 is rated to drive a minimal load of 1 kΩ. However, you can achieve optimal performance with larger load resistances such as 10 kΩ or 100 kΩ. Refer to the *NI USB-443x Specifications* and *NI 446x Specifications* for more information.

Analog Output Channel Configurations

The NI 4461 supports two terminal configurations for analog output: differential and pseudodifferential. The term pseudodifferential refers to the fact that there is a 50 Ω resistor between the outer connector shell and chassis ground. The NI USB-4431 only supports pseudodifferential.

Note Attach PXI/PXIe, and PCI devices to the chassis with screws to provide a reliable ground connection. If you are using a PXI/PXIe device, be sure to tighten the screws at the top and bottom of the front face of the device. If you are using a PCI device, keep the screw that held the PCI slot cover to the computer chassis. Reinsert this screw to securely attach the device. For USB-4431 devices, connect the ground terminal on the back of the USB case to the chassis of the host PC.

Choosing Channel Configurations

If the DUT inputs are floating, use either the pseudodifferential or differential configuration.

If the DUT inputs are grounded or ground referenced, use the differential configuration. Using the pseudodifferential output configuration on a grounded DUT creates more than one ground-reference point. This condition may allow ground loop currents which can introduce errors or noise into the measurement. The 50 Ω or 1 kΩ resistor between the negative input and ground is usually sufficient to reduce these errors to negligible levels, but results can vary depending on your system setup.

Configure the channels based on the signal source reference or DUT configuration. Refer to Table 2-3 to determine how to configure the channel.

Table 2-3. Analog Output

DUT Input Reference	Channel Configuration
Floating	Pseudodifferential or Differential
Grounded	Differential

The NI 446*x* is automatically configured for differential mode when powered on or powered off. This configuration protects the 50 Ω resistor on the negative pin.

Output Impedance

NI 4461

The differential output impedance between positive and negative signal legs is approximately 22 Ω when you generate a waveform. When you are not generating a waveform, configure the AO.IdleOutputBehavior property for one of the idle behavior options listed in Table 2-4.

Table 2-4. Output Impedance

Idle Behavior Option	Output Impedance (Differential Mode Only)
`Maintain Existing Value`	22 Ω
`Zero Volts`	22 Ω
`High Impedance`	9 kΩ

NI USB-4431

The differential output impedance between positive and negative signal legs is approximately 50 Ω. There is no high impedance idle output channel configuration for the NI USB-4431. However the output can be configured to maintain its existing value when idle or return to zero when idle.

DAC

The delta-sigma DACs on the NI 4461 and NI USB-4431 function in a way analogous to delta-sigma ADCs. The digital data first passes through a digital interpolation filter, then to the DAC resampling filter, and finally to the delta-sigma modulator.

In the DAC, the delta-sigma modulator converts high-resolution digital data to high-rate, 1-bit digital data. As in the ADC, the modulator frequency shapes the quantization noise so that almost all of the quantization noise energy is above the Nyquist frequency.

The digital 1-bit data is then passed to an inherently linear 1-bit DAC. The output of the DAC includes quantization noise at higher frequencies, and some images still remain near multiples of eight times the effective sample rate.

Analog Output Filters

Anti-Imaging and Interpolation Filters

A sampled signal repeats itself throughout the frequency spectrum, as shown in Figure 2-2. This figure shows how the signal repetitions begin above one-half the sample rate, f_s, and, theoretically, continue up through the spectrum to infinity. Images remain in the sampled data because the data actually represents only the frequency components below one-half f_s (the baseband). The device filters out the extra images in the signal in three stages.

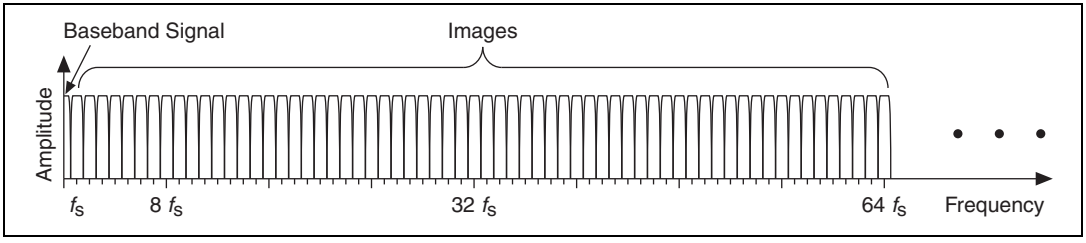

Figure 2-2. Sampled Signal

First, the data is digitally interpolated by a factor of 2^n, where n is a positive integer from 0 to 6 (NI 443*x*) or 0 to 7 (NI 446*x*). Therefore, the effective sample rate (f_{es}) is 2^n x f_s. The interpolation factor must be sufficient to move the effective sample rate into the 51.2 kS/s or higher range (NI 443*x*) or the 102.4 kS/s or higher range (NI 446*x*). Figure 2-3 shows an example of four-times interpolation and the resulting images. A linear-phase digital filter then removes almost all energy above one-half f_s.

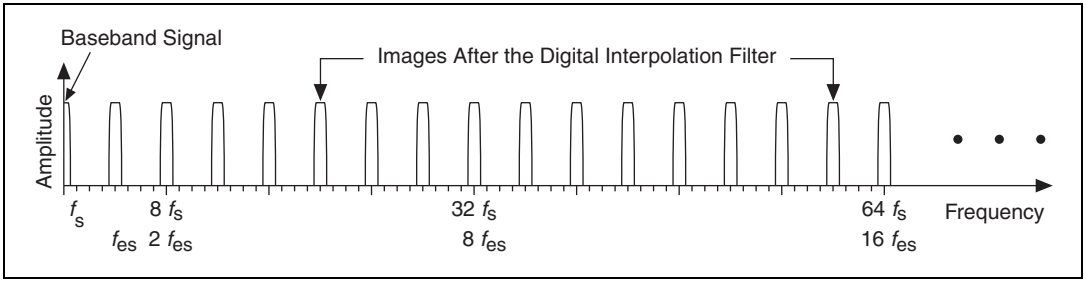

Figure 2-3. Signal After Digital Filter

Second, the DAC resamples the data to a new frequency (f_{DAC}). The frequency f_{DAC} is eight times higher than f_{es}. Figure 2-4 shows the resulting images.

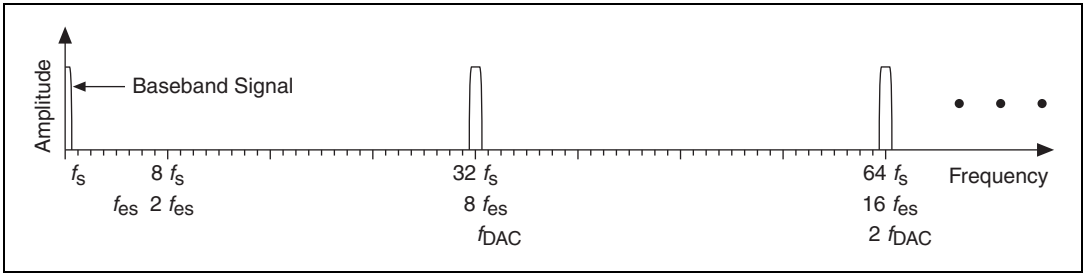

Figure 2-4. Images After DAC Filter

Some further (inherent) filtering occurs at the DAC because the data is digitally sampled and held at eight times f_{es}. This filtering has a sinx/x response, yielding nulls at multiples of eight times f_s, as shown in Figure 2-5.

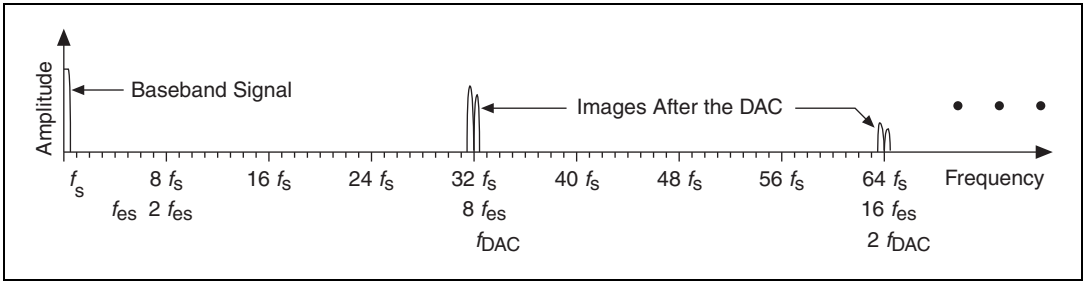

Figure 2-5. Signal After DAC

Third, a multi-pole analog filter with a fixed cut-off at 89 kHz (NI 4431) or 243 kHz (NI 4461) filters the remaining images, as shown in Figure 2-6.

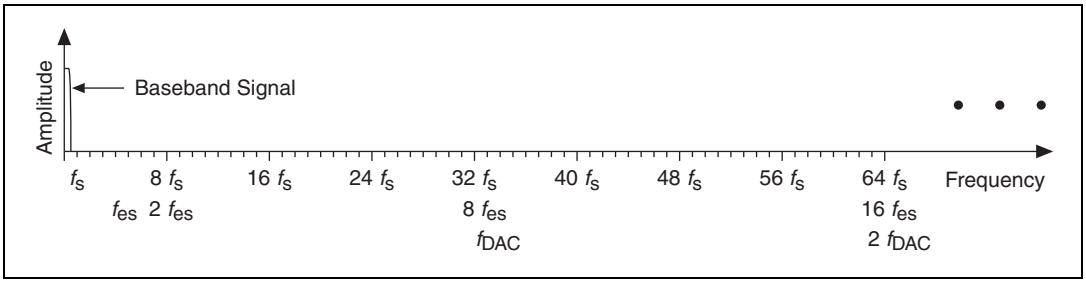

Figure 2-6. Signal After Analog Filters

Filter Delay

Output filter delay—the time required for digital data to propagate through the DAC and interpolation digital filters—varies depending on the update rate for DACs. For example, the filter delay at 10 kS/s for the NI 4461 is 38.5 update clock cycles. This signal experiences a delay equal to 3.85 ms. This delay is an important factor for stimulus-response measurements, control applications, or any application where loop time is critical. You often might want to maximize the sample rate to minimize the time required for a specific number of update clock cycles to elapse, since it varies with frequency, as shown in Table 2-5 and Table 2-6.

The interpolation filter adds additional output filter delay depending on the update rate. Table 2-5 and Table 2-6 provide more information about how the interpolation filter affects the output filter delay.

Table 2-5. NI 4461 Interpolation Factor and Output Filter Delay

Update Rate (kS/s)	Interpolation Factor	NI 4461 Output Filter Delay (Samples)
$1.0 \le f_s \le 1.6$	128	36.6
$1.6 < f_s \le 3.2$	64	36.8
$3.2 < f_s \le 6.4$	32	37.4
$6.4 < f_s \le 12.8$	16	38.5
$12.8 < f_s \le 25.6$	8	40.8
$25.6 < f_s \le 51.2$	4	43.2
$51.2 < f_s \le 102.4$	2	48.0
$102.4 < f_s \le 204.8$	1	32.0

Table 2-6. NI 4431 Interpolation Factor and Output Filter Delay

Update Rate (kS/s)	Interpolation Factor	NI 4461 Output Filter Delay (Samples)
$0.8 \le f_s < 1.6$	64	63.3
$1.6 \le f_s < 3.2$	32	62.6
$3.2 \le f_s < 6.4$	16	61.3
$6.4 \le f_s < 12.8$	8	58.5
$12.8 \le f_s < 25.6$	4	53
$25.6 \le f_s < 51.2$	2	42
$51.2 \le f_s \le 102.4$	1	20

FIFO and PCI Data Transfer

DSA device input channels share a FIFO buffer, and the output channels share a separate FIFO buffer. The *NI USB-443x Specifications* and *NI 446x Specifications* contain information about the buffer sample depth.

The NI 4461 has a flexible data transfer request condition. You can program the device to request DMA transfers according to a programmable FIFO condition. Refer to the *NI-DAQmx Help* or the *LabVIEW Help* for information about conditions available for specific devices.

Note USB devices do *not* support setting the transfer request condition.

Power Off and Power Loss

When the NI 4461 is powered off or loses power, the output channels assume a high-impedance state. The outputs of the NI 4461 drop to 0.0 V in approximately 8 µs. Figure 2-7 illustrates the typical behavior of an NI 4461 generating 10 V when powered off or when the device loses power.

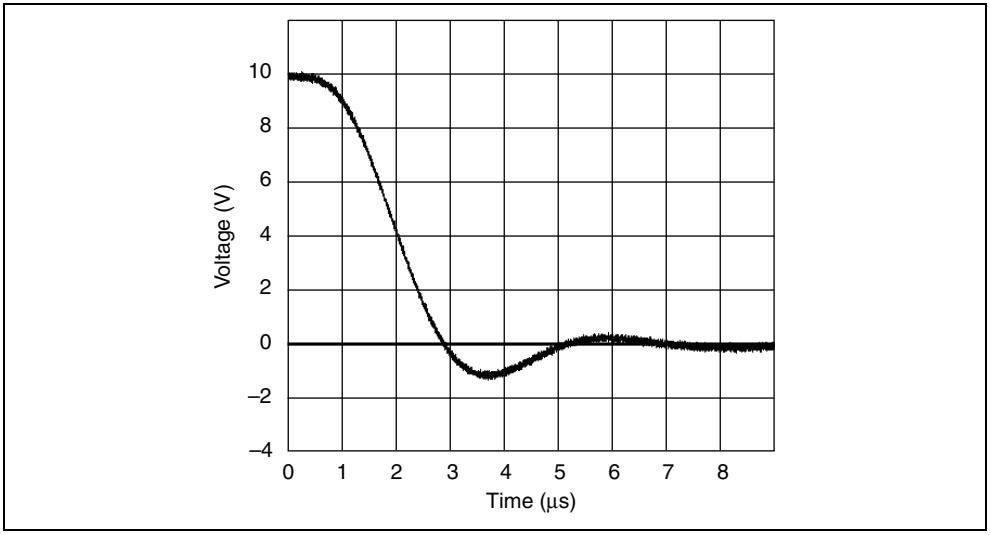

Figure 2-7. Power Off and Power Loss Behavior

Triggering

DSA devices support two types of triggers: start triggers and reference triggers.

- When a DSA device is configured to use a start trigger, the returned data consists of samples that were acquired after the start trigger occurred.
- When a DSA device is configured to use a reference trigger, the returned data consists of samples that were acquired both before and after the trigger. Samples acquired before the reference trigger are called pretrigger samples, and samples acquired after the reference trigger are called posttrigger samples.

For example, a DSA device can be configured to use a digital start trigger, an analog reference trigger, and to acquire 100 pretrigger and 200 posttrigger samples. In this case, the device will start acquiring data after the digital start trigger occurs. It will acquire at least 100 samples, and then begin looking for the analog reference trigger. After the reference trigger occurs, the device will acquire 200 samples, and then stop. The returned data will consist of the 100 samples that occurred before the reference trigger, and the 200 samples that occurred after the reference trigger. Use the NI-DAQmx Trigger VIs to configure trigger properties.

The start and reference triggers can be configured independently, and can be set to use a variety of sources, both analog and digital. Triggers can be configured to occur on either the rising or falling edge of a signal. Moreover, analog triggers support other modes of operation, including triggering on edges with hysteresis, and triggering when a signal enters or leaves a predefined window. Since the start and reference triggers are configured independently, alternate edges of a single signal can be used to control an acquisition or generation.

During repetitive triggering on a waveform, you might observe jitter because of the uncertainty of where a trigger level falls compared to the actual digitized data. Although this trigger jitter is never greater than one sample period, it might be significant when the sample rate is only twice the bandwidth of interest. This jitter usually has no effect on data processing, and you can decrease this jitter by sampling at a higher rate.

Digital Triggering

You can configure DSA devices to trigger in response to a digital signal on the PFI 0 connector, located on the device front panel. This pin is labeled EXT TRIG on NI 447*x* devices, and it is labeled PFI0 on NI 446*x* and NI 449*x* devices. The trigger circuit can respond either to a rising or a falling edge. The trigger signal must comply to TTL voltage levels. Refer to the *NI USB-443x Specifications, NI 446x Specifications*, *NI 447x Specifications*, and *NI 449x Specifications* for additional trigger requirements.

PXI and PCI DSA devices also offer digital triggering in response to signals on the PXI/PXIe or RTSI trigger bus. Use any line from PXI_Trig<0..6> or RTSI<0..6>. One exception applies—when synchronizing multiple NI PXI-447*x* devices, PXI_Trig 5 is reserved for internal use. As with external digital triggering, you can program the device to respond to either the rising or falling signal edge.

Note The NI USB-443*x* devices have eight PFI lines for triggering. These PFI lines are located on the back of the device.

Analog Triggering

You can configure the DSA device analog trigger circuitry to monitor any input channel from which you acquire data. Choosing an input channel as the trigger channel does not influence the input channel acquisition capabilities.

The trigger circuit generates an internal digital trigger based on the input signal and the defined trigger levels. For example, you can configure the device to start acquiring samples after the input signal crosses a specific threshold. You also can route this internal trigger to the PXI/PXIe or RTSI trigger bus to synchronize the start of the acquisition operation by one device with the operation of other devices in the system.

You can use several analog triggering modes with DSA devices, including analog edge, analog edge with hysteresis, and window triggering.

Analog Edge Triggering

For analog edge triggering, configure the device to detect a certain signal **Level** and slope, either rising or falling. Figure 2-8 shows an example of rising edge analog triggering. The trigger asserts when the signal starts below **Level** and then crosses above **Level**.

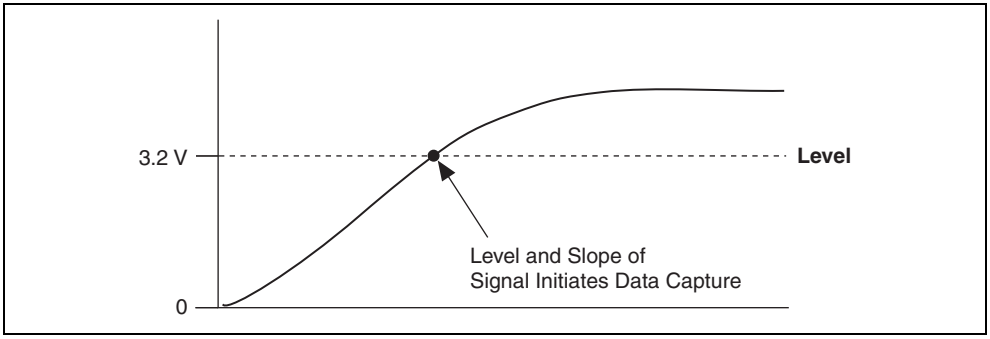

Figure 2-8. Analog Trigger Level

Analog Edge Triggering With Hysteresis

When you add hysteresis to analog edge triggering, you add a window above or below the trigger level. This trigger often is used to reduce false triggering due to noise or jitter in the signal. For example, if you add a hysteresis of 1 V to the example in Figure 2-8, which uses a level of 3.2 V, the signal must start at or drop below 2.2 V to arm the trigger. The trigger asserts when the signal rises above 3.2 V and deasserts when it falls below 2.2 V, as shown in Figure 2-9.

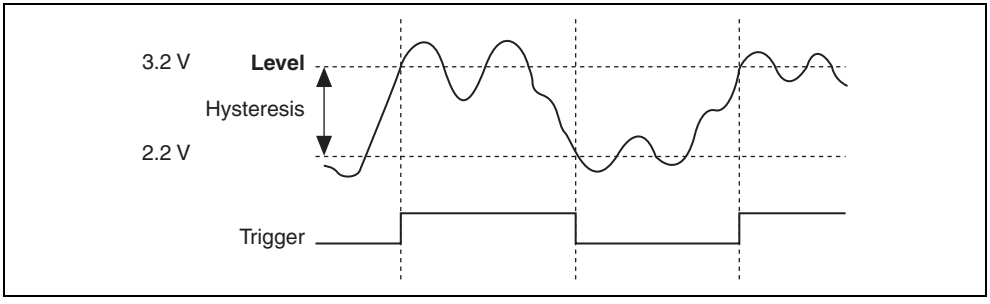

Figure 2-9. Analog Edge Triggering with Hysteresis on Rising Slope

When using hysteresis with a falling slope, the trigger is armed when the signal starts above **Level**, plus the hysteresis value, and asserts when the signal crosses below **Level**. For example, if you add a hysteresis of 1 V to a level of 3.2 V, the signal must start at or rise above 4.2 V to arm the trigger. The trigger asserts as the signal falls below 3.2 V and deasserts when it rises above 4.2 V, as shown in Figure 2-10.

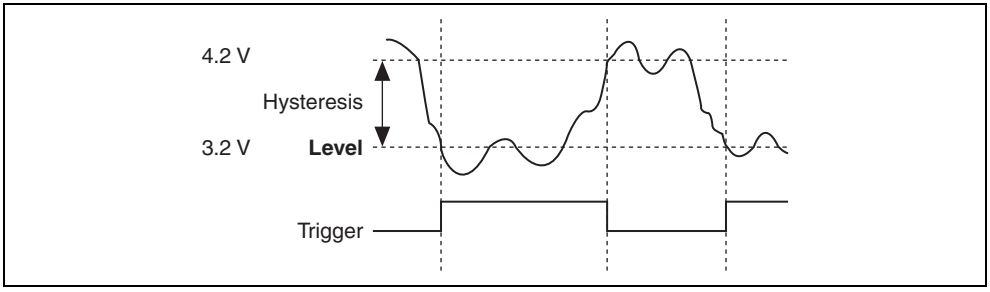

Figure 2-10. Analog Edge Triggering with Hysteresis on Falling Slope

Window Triggering

A window trigger occurs when an analog signal either passes into (enters) or passes out of (leaves) a window defined by two levels. Specify the levels by setting a value for the top and bottom window boundaries. Figure 2-11 demonstrates a trigger that acquires data when the signal enters the window. You can also program the trigger circuit to acquire data when the signal leaves the window.

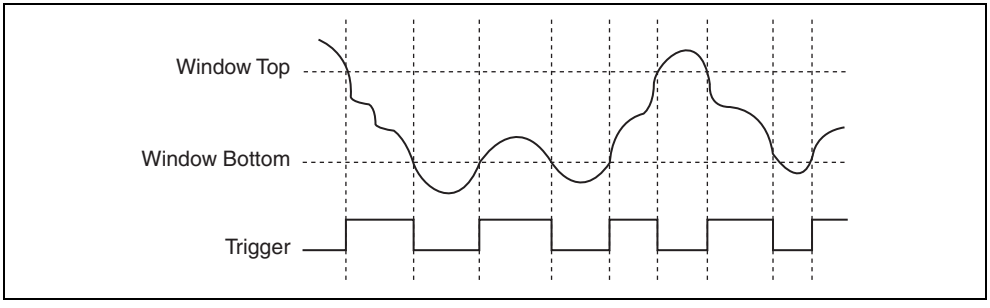

Figure 2-11. Window Triggering

Triggering and Filter Delay

Analog and digital triggering exhibit different behaviors with respect to the filter delay in the ADC.

When you use digital triggering, the ADCs begin generating digital data immediately after receiving the digital trigger signal. However, the analog signal entering the ADCs is still

subject to the filter delay. This circumstance means that when the trigger is received, the analog levels at the front of the ADCs are not digitized until a certain number of sample intervals later. You can observe this behavior with an experiment. Connect the same TTL signal to the external digital trigger input and to an AI channel. Configure the acquisition to respond to a digital trigger. The rising edge of the trigger does not appear in the digitized waveform until a specific number of filter delay samples pass. Refer to the *NI USB-443x Specifications*, *NI 446x Specifications*, *NI 447x Specifications*, and *NI 449x Specifications* for more information about filter delay.

Analog triggering is performed on the digital output of the ADC. The analog trigger circuit on a DSA device is a digital comparator. Because the trigger is located after the ADC in the signal path, the filter delay is not evident in the acquired data. If the analog trigger is configured with a rising edge and a level of 1.0 V, the voltage of the first sample is just above 1.0 V.

Note **(NI USB-4431 and NI 4461)** You must also consider the AO filter delay in your application. The digital filter introduces a deterministic delay during AO operations.

Filter Delay Removal

NI 449*x* devices support the AI.RemoveFilterDelay property. When this feature is enabled, the NI 449*x* device will automatically compensate for the filter delay of its analog input path.

Note The AI.RemoveFilterDelay property cannot be used with an analog start trigger.

Suppose you have configured an NI 449*x* to sample at 204.8 kS/s, and to respond to a digital start trigger. At this sample rate, the filter delay is 64 samples. Without the filter delay removal feature, the first sample will appear to have been acquired roughly 64 samples before the start trigger. With the filter delay removal feature, the first sample is acquired within roughly one sample period of the start trigger.

The AI.RemoveFilterDelay property is especially useful when synchronizing NI 449*x* devices to other data acquisition devices that do not exhibit filter delay. With the filter delay removal feature enabled, the data acquired from all synchronized devices is aligned to within roughly one sample period.

If synchronizing multiple NI 449*x* devices, the filter delay removal feature must be enabled on all of them. Otherwise, the acquired data will not be aligned.

There is a caveat with the filter delay removal feature that comes into play when using an analog reference trigger, and synchronizing to another device by exporting the sample clock (for example, an NI X Series device). In this case, manually add the filter delay of the NI 449*x* device (rounded down to an integer) to the requested pretrigger samples, and subtract it from the posttrigger samples, of all devices importing the NI 449*x* sample clock. If this step is not performed, the devices importing the sample clock will never complete their acquisitions.

Timing and Synchronization

Timing Signals

Frequency Timebase

DSA devices have high-accuracy oscillators on board. The oscillator feeds a direct digital synthesis (DDS) chip, which is used to generate the other on-board timing signals.

Reference Clock

PXI/PXIe chassis backplanes provide a common, 10 MHz reference clock to each peripheral slot. An independent buffer drives the clock signal to each device in the chassis.

DSA devices that support reference clock synchronization are able to lock their frequency timebases to this shared reference.

You can drive PXI_CLK10 from an external source through the PXI_CLK_IN pin on the P2 connector of the star trigger slot on the chassis. Driving an external clock source on this pin automatically disables the 10 MHz source generated on the PXI/PXIe backplane.

Oversample Clock

The delta-sigma converters used on DSA devices acquire 1-bit samples at a rate that is much faster than the requested sample rate. The resulting 1-bit data stream is converted to a 24-bit data stream at the requested sample rate. The oversample clock drives the acquisition of 1-bit samples from the delta-sigma converter. The frequency of the oversample clock is a multiple of the requested sample rate.

Sample Clock Timebase

The sample clock timebase is the timing signal that is used to produce the oversample clock on DSA devices. All of the converters on a single DSA device share a common sample clock timebase.

When a DSA device is operating stand-alone (without synchronizing to other devices), a DDS chip produces the sample clock timebase. DDS is a method of generating a programmable clock with excellent frequency resolution.The DDS chips are capable of between 28- and 32-bits of resolution, and can produce between 2^{28} and 2^{32} frequency steps to create the sample clock timebase.

When synchronizing multiple DSA devices, each device must share a common sample clock timebase. When multiple devices share a common sample clock timebase, each is able to generate a phase-aligned version of the ADC and DAC oversample clocks. This allows for

tight synchronization between multiple devices. There are two methods available to share a common sample clock timebase:

- Generate the sample clock timebase on a master device. Route the generated timebase to all slave devices. Refer to the *Master Sample Clock Timebase Synchronization* section in this chapter for more information.
- Configure each DSA device to generate its own sample clock timebase. Lock the frequency timebase on each device to the reference clock provided by the backplane. At this point, a sync pulse can be distributed to each device. This will automatically phase-align the generated sample clock timebase on each device. Refer to the *Reference Clock Synchronization (PXI/PXIe Only)* section in this chapter for more information.

The ratio between the sample rate (f_s) and sample clock timebase rate (f_{tb}) can have one of several values. Refer to the *NI 446x Specifications*, *NI 447x Specifications*, *NI 449x Specifications,* or *NI USB-443x Specifications* for more information.

The sample clock timebase has stringent requirements for frequency and stability. DSA devices do not accept arbitrary clock signals from external sources such as encoders or tachometers. However, signal processing features in the Sound and Vibration Measurement Suite often provide an excellent alternative to external clocking in encoder and tachometer applications. Visit `ni.com/soundandvibration` for more information about the Sound and Vibration Measurement Suite.

Note **(NI USB-4431 and NI 4461)** You can run input and output operations simultaneously at different rates on the NI USB-4431 and NI 4461. However, because the timing information for all operations is derived from a common sample clock timebase, the ratio between every input and output rate must be a power of 2. For example, assume that the input sample rate is 8 kS/s. Valid output update rates include, but are not limited to, 2 kS/s, 8 kS/s, 16 kS/s, and 64 kS/s. In this case, 20 kS/s is not a valid output update rate, because the ratio between 8 kS/s and 20 kS/s is not a power of 2.

Sync Pulse

The sync pulse is used with DSA synchronization. It has two purposes:

- It resets the DDS chips and clock dividers on each DSA device at the same instant. This aligns the sample clock timebase signals (when using reference clock synchronization) and the oversample clocks on each device.
- It resets the ADCs and DACs on each DSA device at the same instant. This aligns the ADCs and DACs.

When synchronizing multiple DSA devices, one device must export a sync pulse, and all other devices must import it. This allows each device in the system to be reset simultaneously.

Start Trigger

When synchronizing multiple DSA devices, each device must start acquiring (and generating) data simultaneously. To align the acquisition and generation events, one device must export a start trigger, and all other devices must import it.

Sample Rate and Update Rate, Accuracy and Coercion

On DSA devices, a DDS chip produces the sample clock timebase. DDS is a method of generating a programmable clock with excellent frequency resolution. The DDS chip takes as an input another higher frequency clock called the frequency timebase. All of the timing signals on a device are derived from the sample clock timebase.

When using a DSA device, you specify the sample and update rates that the device will use when acquiring and generating samples. However, the device will never run at exactly the rate you request. The difference between the requested rate and the actual rate depends on two factors:

- The accuracy of the frequency timebase (the input to the DDS chip)
- The frequency resolution of the DDS chip

The accuracy of the frequency timebase usually dominates the frequency resolution of the DDS chip, especially if the internal frequency timebase is used. However, in some applications, it is useful to understand the effect of the frequency resolution of the DDS chip.

Suppose that the frequency timebase on a DSA device has no error. There will still be a small error between the actual and requested rates, because DDS chips do not have unlimited frequency resolution. For example, if you request that an NI 4461 acquire data at 200 kS/s, NI-DAQmx automatically coerces the sample rate to a slightly higher value of 200.0000000407 kS/s. This process is transparent, although NI-DAQmx allows you to query the coerced sample or update rate by reading the SampClk.Rate NI-DAQmx Timing property. The returned value does not take into account errors in the frequency timebase. To calculate the rate, follow the procedure in the *Calculating the Coerced Rate* section.

Calculating the Coerced Rate

To calculate the coerced rate, use the following steps:

1. Calculate the frequency of the sample clock timebase (the DDS chip output) needed to run at the requested rate.
2. Calculate the value of the tuning word needed to run at the requested rate. The tuning word is a 28- or 32-bit integer that is programmed into the DDS chip in order to set the desired sample clock timebase frequency. In almost all cases, the calculated tuning word is not an integer. This signifies that the DDS chip cannot generate the exact sample clock timebase frequency that is needed to run at the requested rate. In this case, NI-DAQmx

rounds the calculated tuning word to the next highest integer. Therefore, the coerced rate is slightly higher than the requested rate.

3. Using the rounded tuning word, calculate the actual frequency of the sample clock timebase.
4. Using the actual frequency of the sample clock timebase, calculate the actual rate that the DSA device will use when acquiring or generating samples.

Calculate the Frequency of the Sample Clock Timebase

Use Table 2-7, 2-8, 2-9, or 2-10 to determine the rate multiplier. The rate multiplier depends on the desired rate, the device being used, and, if using an NI 447*x*, whether enhanced low-frequency alias rejection is enabled. The rate multiplier is also used to calculate the actual sample or update rate. Refer to the *Calculate the Actual Sample or Update Rate* section.

Table 2-7. Rate Multipliers for NI 443*x*

Rate (kS/s)	Rate Multiplier
$0.8 \le f_s < 1.6$	2^{15}
$1.6 \le f_s < 3.2$	2^{14}
$3.2 \le f_s < 6.4$	2^{13}
$6.4 \le f_s < 12.8$	2^{12}
$12.8 \le f_s < 25.6$	2^{11}
$25.6 \le f_s < 51.2$	2^{10}
$51.2 \le f_s \le 102.4$	2^{9}

Table 2-8. Rate Multipliers for NI 446*x*

Rate (kS/s)	Rate Multiplier
$1.0 \le f_s \le 1.6$	2^{14}
$1.6 < f_s \le 3.2$	2^{13}
$3.2 < f_s \le 6.4$	2^{12}
$6.4 < f_s \le 12.8$	2^{11}
$12.8 < f_s \le 25.6$	2^{10}
$25.6 < f_s \le 51.2$	2^{9}

Table 2-8. Rate Multipliers for NI 446*x* (Continued)

Rate (kS/s)	Rate Multiplier
$51.2 < f_s \leq 102.4$	2^8
$102.4 < f_s \leq 204.8$	2^7

Table 2-9. Rate Multipliers for NI 447*x*

Rate (kS/s)	Rate Multiplier	Rate Multiplier, Enhanced Alias Rejection Enabled
$1.0 \leq f_s \leq 1.6$	2^8	2^{13}
$1.6 < f_s \leq 3.2$	2^8	2^{12}
$3.2 < f_s \leq 6.4$	2^8	2^{11}
$6.4 < f_s \leq 12.8$	2^8	2^{10}
$12.8 < f_s \leq 25.6$	2^8	2^9
$25.6 < f_s \leq 51.2$	2^8	—
$51.2 < f_s \leq 102.4$	2^7	—

Table 2-10. Rate Multipliers for NI 449*x*

Rate (kS/s)	Rate Multiplier
$0.1 \leq f_s \leq 0.2$	2^{17}
$0.2 < f_s \leq 0.4$	2^{16}
$0.4 < f_s \leq 0.8$	2^{15}
$0.8 < f_s \leq 1.6$	2^{14}
$1.6 < f_s \leq 3.2$	2^{13}
$3.2 < f_s \leq 6.4$	2^{12}
$6.4 < f_s \leq 12.8$	2^{11}
$12.8 < f_s \leq 25.6$	2^{10}
$25.6 < f_s \leq 51.2$	2^9

Table 2-10. Rate Multipliers for NI 449*x* (Continued)

Rate (kS/s)	Rate Multiplier
$51.2 < f_s \leq 102.4$	2^8
$102.4 < f_s \leq 204.8$	2^7

Refer to Equation 2-1 to determine the frequency of the sample clock timebase.

$$SampTimebaseRate = Rate \times RateMultiplier \quad (2\text{-}1)$$

where

Rate is the desired sample or update rate.

RateMultiplier is the rate multiplier value from Tables 2-7 through 2-10.

Calculate the DDS Tuning Word

Determine the frequency of the frequency timebase (the input clock to the DDS), the number of bits in the DDS, and the size of the external clock multiplier on the device being used by using Table 2-11. These values are also used in the *Calculate the Actual Frequency of the Sample Clock Timebase* section.

Table 2-11. Clock Properties On DSA Devices

Device	Nominal Frequency of Frequency Timebase (MHz)	Number of DDS Bits	External Clock Multiplier
NI 443*x*	48.0	28	6
NI 446*x*	100.0	32	1
NI 447*x*	104.8576		
NI 449*x*	100.0		

Refer to Equation 2-2 to determine the DDS tuning word.

$$TuningWord = ceiling\left(\frac{SampTimebaseRate}{ExternalMult} \times \frac{2^{DdsBits}}{FreqTimebaseRate}\right) \quad (2\text{-}2)$$

where

SampTimebaseRate is the frequency of the sample clock timebase (calculated in the *Calculate the Frequency of the Sample Clock Timebase* section).

ExternalMult, *DdsBits*, and *FreqTimebaseRate* are the values from Table 2-11.

The ceiling function rounds a number to the next highest integer. For example, ceiling(1.1) = 2, and ceiling(2.0) = 2.

Calculate the Actual Frequency of the Sample Clock Timebase

Refer to Equation 2-3 to determine the actual frequency of the sample clock timebase.

$$ActSampTimebaseRate = \frac{TuningWord}{2^{DdsBits}} \times FreqTimebaseRate \times ExternalMult \quad (2\text{-}3)$$

where

TuningWord is the DDS tuning word that was calculated in the *Calculate the DDS Tuning Word* section.

ExternalMult, *DdsBits*, and *FreqTimebaseRate* are the values from the Table 2-11.

Calculate the Actual Sample or Update Rate

Refer to Equation 2-4 to determine the actual sample or update rate.

$$ActRate = \frac{ActSampTimebaseRate}{RateMultiplier} \quad (2\text{-}4)$$

where

ActSampTimebaseRate is the actual sample clock timebase rate calculated in the *Calculate the Actual Frequency of the Sample Clock Timebase* section.

RateMultiplier is the rate multiplier value from Tables 2-7 through 2-10.

Example of Calculating a Coerced Sample Rate

Table 2-12 lists the rates that different DSA devices will actually sample at if configured to run at one of several different rates. This assumes that the frequency timebase is running at exactly the nominal rate.

Table 2-12. Coerced Sample and Update Rates on DSA Devices (kS/s)

Desired Rate (kS/s)	DSA Device			
	NI 443*x*	**NI 446*x***	**NI 447*x***	**NI 449*x***
1.0	1.0000000111	1.000000000317	1.0	1.000000000317
20.0	20.000000484	20.0000000177	20.0	20.0000000177

Table 2-12. Coerced Sample and Update Rates on DSA Devices (kS/s) (Continued)

Desired Rate (kS/s)	DSA Device			
	NI 443*x*	**NI 446*x***	**NI 447*x***	**NI 449*x***
80.0	80.00000194	80.0000000709	80.0	80.0000000709
100.0	100.000000326	100.0000000204	100.0	100.0000000204

Equations 2-5 through 2-8 show how a 1 kS/s sample rate on an NI 4461 is coerced to a slightly higher value.

Calculate the Frequency of the Sample Clock Timebase

From Table 2-8, the rate multiplier at the 1 kS/s sample rate is 2^{14}. Therefore, the frequency of the sample clock timebase is:

$$SampTimebaseRate = Rate \times RateMultiplier = 1\ \text{kS/s} \times 2^{14} = 16.384\ \text{MHz} \quad (2\text{-}5)$$

Calculate the DDS Tuning Word

From Table 2-11, the frequency of the frequency timebase on the NI 4461 is 100.0 MHz, the DDS has 32 bits, and the external clock multiplier is 1. The sample clock timebase frequency calculated in Equation 2-5 is 16.384 MHz when sampling at 1 kS/s. Therefore, the tuning word is:

$$TuningWord = ceiling\left(\frac{SampTimebaseRate}{ExternalMult} \times \frac{2^{DdsBits}}{FreqTimebaseRate}\right) = ceiling\left(\frac{16.384\ \text{MHz}}{1} \times \frac{2^{32}}{100.0\ \text{MHz}}\right) = 703{,}687{,}442 \quad (2\text{-}6)$$

Calculate the Actual Frequency of the Sample Clock Timebase

The frequency of the frequency timebase on the NI 4461 is 100.0 MHz, the DDS has 32 bits, and the external clock multiplier is 1. The tuning word calculated in Equation 2-6 is 703,687,442 when sampling at 1 kS/s. Therefore, the actual frequency of the sample clock timebase is:

$$ActSampTimebaseRate \quad (2\text{-}7)$$
$$= \frac{TuningWord}{2^{DdsBits}} \times FreqTimebaseRate \times ExternalMult$$
$$= \frac{703{,}687{,}442}{2^{32}} \times 100.0\ \text{MHz} \times 1 = 16.38400000520\ \text{MHz}$$

Calculate the Actual Sample or Update Rate

The rate multiplier on the NI 4461 at the 1 kS/s sample rate is 2^{14}. From Equation 2-7, the actual frequency of the sample clock timebase is 16.38400000520 MHz. Therefore, the actual sample rate is:

$$ActRate \quad (2\text{-}8)$$
$$= \frac{ActSampTimebaseRate}{RateMultiplier} = \frac{16.38400000520\ \text{MHz}}{2^{14}} = 1.000000000317\ \text{kS/s}$$

Synchronization

NI-DAQmx can automatically synchronize multiple DSA devices to run at the same rate as each other. Just add channels from multiple devices to the same NI-DAQmx task, and NI-DAQmx will automatically control clock sharing and sync pulse routing.

The following methods show how you can add channels from multiple devices to the same NI-DAQmx task.

- When using the DAQ Assistant, you can select more than one physical channel at a time, or you can click the **Add Channels** button to add additional channels.
- When creating a task programmatically, you can specify a physical channel string containing channels from multiple devices, such as `PXI1Slot2/ai0:7,PXI1Slot3/ai0:7`.
- You can also call the NI-DAQmx Create Channel VI multiple times on the same task, specifying different channels for each call. This allows you to use multiple measurement types, such as acceleration, sound, pressure, and voltage in the same task.

Some applications require tight synchronization between input and output operations on multiple devices. Synchronization is important to minimize skew between channels or to eliminate clock drift between devices in long-duration operations. You can synchronize the analog input and output operations on two or more DSA devices to extend the channel count of DSA measurements. Table 2-13 lists possible DSA device synchronization configurations to help you decide the method of synchronization to use.

Note For information about synchronizing DSA devices with other NI products that are not listed in Table 2-13, refer to the NI Developer Zone at `ni.com/zone`.

Table 2-13. Supported DSA Device Synchronization Configuration

Configuration	Reference Clock (PXI/PXIe Only)	Master Sample Clock Timebase*,†
NI 449*x* and NI 449*x*	Supported	—
NI 446*x* and NI 446*x*	Supported	Supported
NI 447*x* and NI 447*x*	—	Supported
NI 449*x* and NI 446*x*	Supported	—
NI 449*x* and NI 447*x*	—	—
NI 446*x* and NI 447*x*‡, **	—	Supported
NI 449x and NI 433x††	Supported	—

* DSA devices with an eHM (PXI hybrid compatible) backplane connector do not support master sample clock timebase synchronization.

† When using master sample clock timebase synchronization in a PXIe chassis, all DSA devices must be slaves. A timing module capable of driving the PXI Star and trigger lines must be the master.

‡ Multirate synchronization is not supported.

** The NI 446*x* must be the master DSA device.

†† NI-DAQmx 9.1 and later support synchronizing NI PXIe-4330/4331 bridge devices with NI PXIe-449*x* devices using reference clock synchronization. The NI PXIe-4330/4331 must be the master device.

Note: NI USB-443*x* devices do not support synchronization.

Refer to Chapter 3, *Developing Your Dynamic Signal Acquisition Application*, for more information about developing synchronization applications with DSA devices.

Reference Clock Synchronization (PXI/PXIe Only)

With reference clock synchronization, master and slave devices lock their frequency timebases (the inputs of their DDS chips) to the PXI_CLK10 signal (the 10 MHz clock supplied by the PXI/PXIe backplane). This is accomplished by using phase-locked loop (PLL) circuitry. After the inputs of the DDS chips on each device are phase-aligned, a sync pulse is sent, which aligns the sample clock timebase on each device (the output of each DDS chip), the oversample clocks, and the ADCs and DACs. Finally, a shared start trigger is sent, which starts the acquisition and generation events on each device at the same instant.

When using this method of synchronization, master and slave devices can be placed in any slot in the PXI/PXIe chassis. You can synchronize all devices in the chassis.

After you install the DSA devices in the chassis, complete these steps to synchronize the hardware:

1. Specify PXI_CLK10 as the reference clock source for all devices to force the DSA devices to lock to the reference clock on the PXI/PXIe chassis.
2. Choose an arbitrary master device to issue a sync pulse on one of the PXI/PXIe Trigger lines. The sync pulse aligns all the clocks in the system to within nanoseconds and also resets the ADCs and DACs.
3. Read the SyncPulse.SyncTime NI-DAQmx Timing property on all of the devices that are importing the sync pulse. Calculate the maximum value, and write it to the SyncPulse.MinDelayToStart NI-DAQmx Timing property on the device that is exporting the sync pulse.
4. Configure one of the DSA devices in the system to export its start trigger on one of the PXI/PXIe trigger lines.

   If possible, configure the device that is exporting the sync pulse to also export the start trigger. However, if the application demands it, separate devices can export the sync pulse and start trigger. In this case, the configuration information for all the devices that are importing the sync pulse must be manually committed prior to starting any of the devices. To manually commit a task, use the NI-DAQmx Control Task VI with a value of *commit* wired to the action control.
5. Start all of the devices that are importing the start trigger by using the NI-DAQmx Start Task VI. Finally, start the device that is exporting the start trigger. This will cause all devices in the system to start acquiring and generating data simultaneously.

Consider the following caveats to using reference clock synchronization:

- Not all DSA devices support low-frequency alias rejection. When you synchronize multiple DSA devices, you must verify that all the devices share the same low-frequency alias rejection setting. You can enable low-frequency alias rejection if all of the DSA devices in the system support it. Disable low-frequency alias rejection on all devices when at least one DSA device does not support it.

- Inherent delays exist between different families of DSA devices. You might need to compensate for filter delay in the waveforms when you synchronize between device families.
- At very low sample rates, you might notice that it takes several seconds for an acquisition to begin. This is because during the sync pulse, the ADCs get reset and require many sample clock cycles before they are operational. The reset process takes longer when slower sample clocks are used. To improve the time it takes an acquisition to begin, select a higher sample rate or enable low-frequency alias rejection on all devices, if possible. This causes the ADCs to run at a higher sample rate, while the onboard firmware decimates the data back to your low sample rate.
- For configurations that specify multiple sample rates between different devices, all rates must be related by a power of two. For example, if one device has a sample rate of 100 kS/s, the other devices can run at 50 kS/s, 25 kS/s, or 200 kS/s but not at 40 kS/s. The slowest running device in the system must export the start trigger. Because the delta sigmas run at different rates, you have different filter delays among all devices running at different rates.

Master Sample Clock Timebase Synchronization

With master sample clock timebase synchronization, one master device exports its master sample clock timebase signal to all the other devices in the system. Next, a sync pulse is sent, which phase-aligns all the oversample clocks on all the devices, as well as the ADCs and DACs. Finally, a shared start trigger is sent, which starts the acquisition and generation events on each device at the same instant.

For a PXI/PXIe system, the master device must reside in the master timebase slot of the chassis, because the master timebase slot has specific point-to-point routing, called PXI Star, to the other peripheral slots on which it exports the clock. For a PXIe chassis, all DSA devices must be slaves. A timing module capable of driving the PXI Star and trigger lines must be the master. A PXI system cannot synchronize devices with master sample clock timebase synchronization beyond slot 14. PXIe systems can synchronize all peripheral slots to the master sample clock timebase. For PCI devices, the clock is physically exported through a RTSI cable that you must attach to the back of all the synchronized devices in the system.

After you install the DSA devices, complete the following steps to synchronize the hardware.

1. Program the master device to export its sample clock timebase to all the slave devices. This shared clock guarantees that all ADC and DAC clocks share the same oversample clock. The signal is routed on PXI Star for PXI/PXIe systems and any of the RTSI lines for PCI systems. The default RTSI line is 8.
2. Program the master device to route a sync pulse to all the slave devices. For PXI/PXIe systems, you can use any of the PXI/PXIe trigger lines to route a sync pulse to all slave devices. For PCI devices, the default RTSI line is 9, but you can program another RTSI

line. The sync pulse aligns all the clocks in the system to within nanoseconds and also resets the ADCs and DACs.

3. Read the SyncPulse.SyncTime NI-DAQmx Timing property on all of the devices that are importing the sync pulse. Calculate the maximum value, and write it to the SyncPulse.MinDelayToStart property on the device that is exporting the sync pulse.
4. Configure one of the DSA devices in the system to export its start trigger on one of the PXI/PXIe trigger lines for a PXI/PXIe system, or one of the RTSI lines 0 to 6 for a PCI system.

   If possible, configure the device that is exporting the sync pulse to also export the start trigger. However, if the application demands it, separate devices can export the sync pulse and start trigger. In this case, the configuration information for all the devices that are importing the sync pulse must be manually committed prior to starting any of the devices. To manually commit a task, use the NI-DAQmx Control Task VI with a value of *commit* wired to the action control.
5. Start all of the devices that are importing a start trigger by using the NI-DAQmx Start Task VI. Finally, start the device that is exporting the start trigger. This will cause all devices in the system to start acquiring and generating data simultaneously.

Consider the following caveats to using master sample clock timebase synchronization:

- Not all DSA devices support low-frequency alias rejection. When you synchronize multiple DSA devices, you must verify that all the devices share the same low-frequency alias rejection setting. You can enable low-frequency alias rejection if all of the DSA devices in the system support it. Disable low-frequency alias rejection on all devices when at least one DSA device does not support it.
- Inherent delays exist between different families of DSA devices. You might need to compensate for filter delay in the waveforms when you synchronize between device families.
- At very low sample rates, you might notice that it takes several seconds for an acquisition to begin. This is because during the sync pulse, the ADCs get reset and require many sample clock cycles before they are operational. The reset process takes longer when slower sample clocks are used. To improve the time it takes an acquisition to begin, select a higher sample rate or enable low-frequency alias rejection on all devices, if possible. This causes the ADCs to run at a higher sample rate, while the onboard firmware decimates the data back to your low sample rate.
- For configurations that specify multiple sample rates between different devices, the rates on all devices must be related by a power of 2. Moreover, the slave devices must not run faster than the master device. For example, if the master device has a sample rate of 100 kS/s, the slave devices can run at 50 kS/s or 25 kS/s, but not at 40 kS/s or 200 kS/s. The slowest running device in the system must export the start trigger. Because the delta-sigmas run at different rates, you have different filter delays among all devices running at different rates.

3

Developing Your Dynamic Signal Acquisition Application

Creating a Task Using the DAQ Assistant

Using the DAQ Assistant to create and configure a task allows you to save several programming steps in your application. In addition, you can save the task for use in future applications. You can use tasks you create with the DAQ Assistant with any NI application software you use to control a DSA device. You can launch the DAQ Assistant from any NI application software.

If you are programming in LabVIEW, you can take advantage of the DAQ Assistant Express VI to further simplify your application. The DAQ Assistant Express VI allows you to perform a complete analog input or analog output operation using a single VI on the LabVIEW block diagram. The DAQ Assistant Express VI uses the DAQ Assistant to create and configure a task and also handles task execution. Refer to the *LabVIEW Help* for more information about the DAQ Assistant Express VI.

Refer to your NI application software documentation for specific information about launching the DAQ Assistant. Refer to the *DAQ Assistant Help* for more information about using the DAQ Assistant.

Analog Input Applications

Analog Input Application Overview

This section presents some general overview information about creating an analog input application using NI-DAQmx and LabVIEW or LabWindows™/CVI™.

Figure 3-1 shows a typical flowchart for programming an analog input task, taking a measurement, and clearing the task.

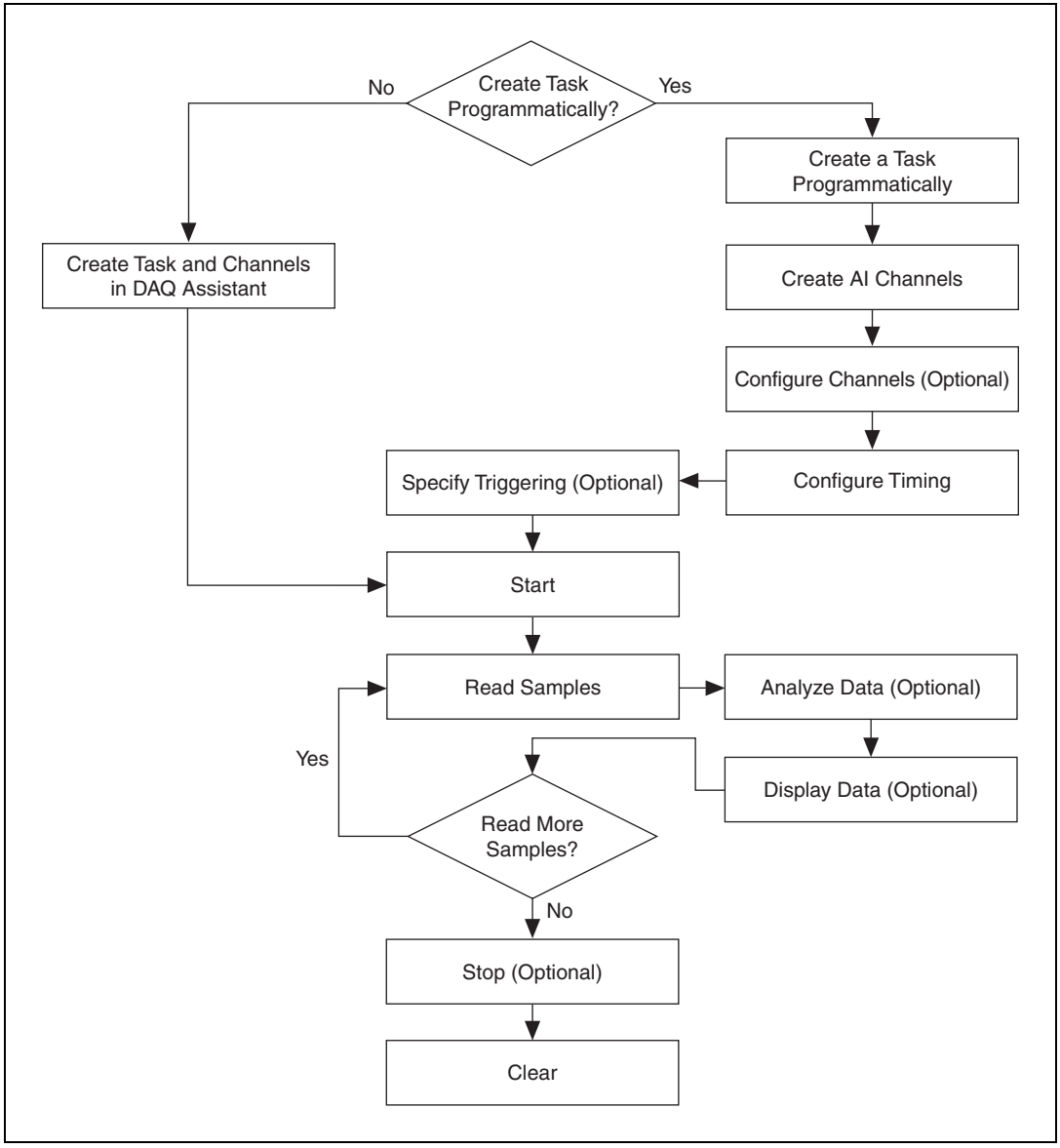

Figure 3-1. Analog Input Task Flowchart

Table 3-1 describes in more detail the steps outlined in Figure 3-1. Some steps might be optional, depending on your application. Refer to your NI application software for more information about each step.

Table 3-1. Analog Input Application Steps

Flowchart Step	LabVIEW Step	LabWindows/CVI Step
Create Task	Create a task using the DAQ Assistant *or* Create a task programmatically using the following VIs: • DAQmx Create Task VI* • DAQmx Create Virtual Channel VI • DAQmx Timing VI • DAQmx Triggering VI*	Create a task using the DAQ Assistant *or* Create a task programmatically using the following functions: • `DAQmxCreateTask` • `DAQmxCreateAIVoltageChan` • `DAQmxCfgSampClkTiming` • `DAQmxAnlgEdgeStartTrig`* *or* • `DAQmxCfgDigEdgeStartTrig`*
Configure Channels	One or more channel property node(s)†	One or more calls to `DAQmxSetChanAttribute`†
Start Measurement*	DAQmx Start Task VI	`DAQmxStartTask`
Read Measurement	DAQmx Read VI	`DAQmxReadAnalog64` or other data reading function
Analyze Data	Common analysis tools include VIs from the Sound and Vibration Measurement Suite or Waveform Measurement Functions‡	Common analysis tools include the functions in the LabWindows/CVI Advanced Analysis Library‡
Display Data	Front panel graph, chart, or indicator	Graphical User Interface (GUI) graph, chart, or indicator
Continue Sampling	Loop around DAQmx Read VI	Loop around `DAQmxReadAnalog64` or other data reading function
Stop Measurement*	DAQmx Stop Task VI	`DAQmxStopTask`
Clear Task	DAQmx Clear Task VI	`DAQmxClearTask`

* These steps might be optional depending on your application.

† Refer to the *NI-DAQmx Help* or the *LabVIEW Help* for more information about NI-DAQmx properties.

‡ This library requires either the Full or Professional Development System of the NI application software.

Note Table 3-1 provides example functions for LabWindows/CVI. In most cases, LabWindows/CVI code ports directly to other ANSI C environments including Microsoft Visual C++. If you are using other text-based application software, including NI Measurement Studio in a .NET environment, you may need to make minor changes in the function syntax.

Refer to your application software or the *Analog Input Application Examples* section of this chapter to view some example analog input applications.

Analog Input Application Examples

NI-DAQmx and all NI ADEs ship with examples you can use to get started with your application.

LabVIEW Examples

The following LabVIEW examples illustrate common DSA analog input applications:

- Example Acceleration Application—Cont Acq Accel Samples-Int Clk-Analog Start VI located in `labview\examples\DAQmx\Analog In\Measure Acceleration.llb`
- Example Sound Pressure Application—Cont Acq Snd Pressure Samples-Int Clk VI located in `labview\examples\DAQmx\Analog In\Measure Sound Pressure.llb`

LabWindows/CVI Examples

The following LabWindows/CVI examples in the CVI folder illustrate common DSA analog input applications:

- Example Acceleration Application—`samples\DAQmx\Analog In\Measure Acceleration\Cont Accel Samps-Int Clk-Anlg Start`
- Example Sound Pressure Application—`samples\DAQmx\Analog In\Measure Sound Pressure\Cont Acq Snd Press Samps-Int Clk`

Analog Output Applications (NI USB-4431 and NI 4461 Only)

Analog Output Application Overview

This section presents some general overview information about creating an analog output application using NI-DAQmx and LabVIEW or LabWindows/CVI.

Figure 3-2 shows a typical flowchart for programming an analog output task, generating a waveform, and clearing the task.

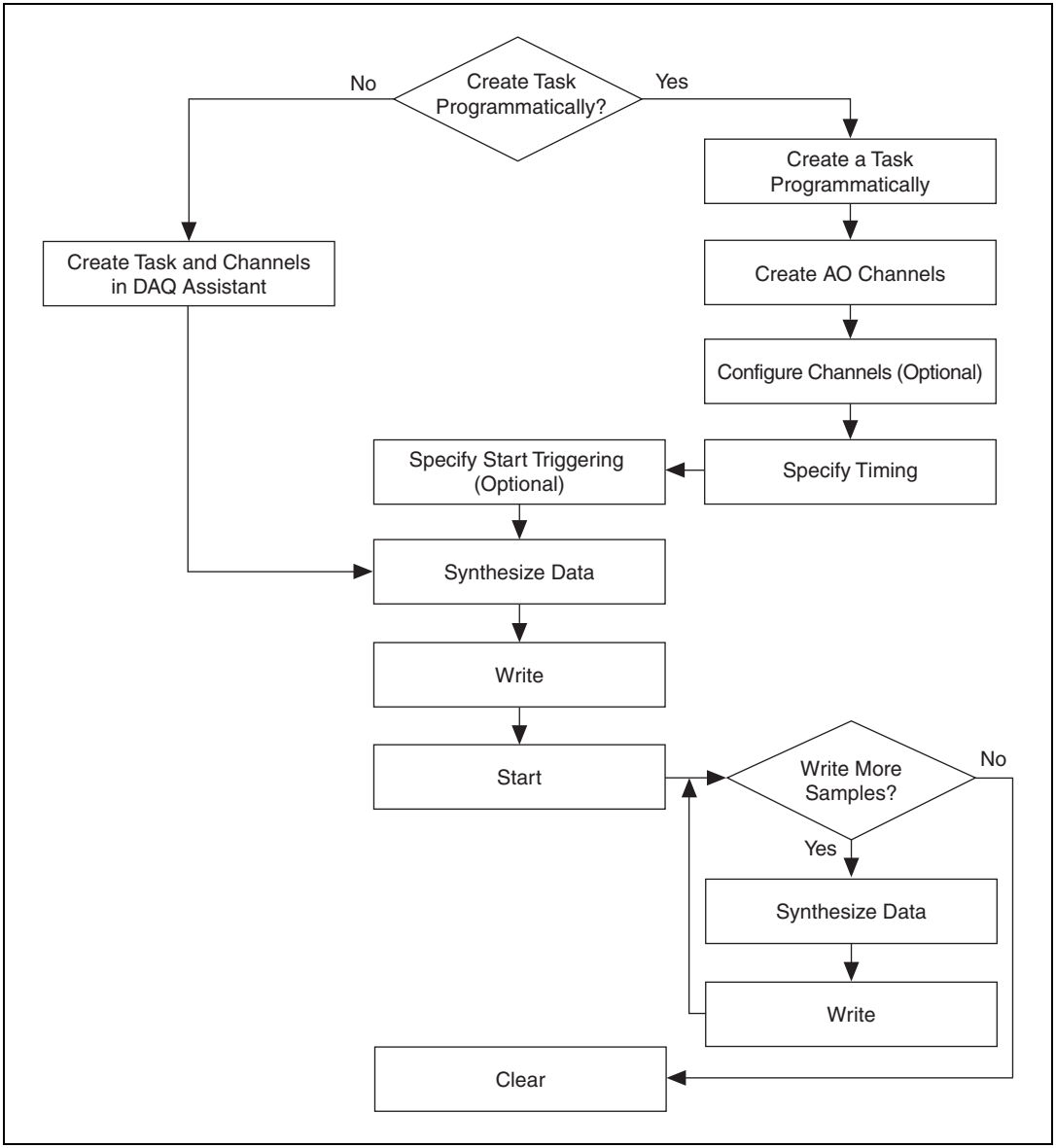

Figure 3-2. NI USB-4431 and NI 4461 Analog Output Task Flowchart

Table 3-2 describes in more detail the steps outlined in Figure 3-2. Some steps might be optional, depending on your application. Refer to your NI application software documentation for more information about each step.

Table 3-2. Analog Output Application Steps

Flowchart Step	LabVIEW Step	LabWindows/CVI Step
Create Task	Create a task using the DAQ Assistant *or* Create a task programmatically using the following VIs: • DAQmx Create Task VI* • DAQmx Create Virtual Channel VI • DAQmx Timing VI • DAQmx Triggering VI*	Create a task using the DAQ Assistant *or* Create a task programmatically using the following functions: • `DAQmxCreateTask` • `DAQmxCreateAOVoltageChan` • `DAQmxCfgSampClkTiming` • `DAQmxAnlgEdgeStartTrig`* *or* • `DAQmxCfgDigEdgeStartTrig`*
Configure Channels	One or more channel property node(s)†	One or more calls to `DAQmxSetChanAttribute`
Synthesize Data*	Common tools include VIs from the Sound and Vibration Measurement Suite or Waveform Measurement VIs†	Common analysis tools include the functions in the LabWindows/CVI Advanced Analysis Library†
Write Data	DAQmx Write VI	`DAQmxWriteAnalog64` or other data writing function
Start Generation	DAQmx Start Task VI	`DAQmxStartTask`
Continue Generation*	Loop around data synthesis and DAQmx Write VI	Loop around data synthesis and `DAQmxWriteAnalog64` or other data writing function
Stop Generation*	DAQmx Stop Task VI	`DAQmxStopTask`
Clear Task	DAQmx Clear Task VI	`DAQmxClearTask`

* These steps might be optional depending on your application.

† This library requires either the Full or Professional Development System of the NI application software.

Note Table 3-2 provides example functions for LabWindows/CVI. In most cases, LabWindows/CVI code ports directly to other ANSI C environments including Microsoft Visual C++. If you are using other text-based application software, including NI Measurement Studio in a .NET environment, you might need to make minor changes in the function syntax.

Refer to your application software or the *Analog Output Application Examples* section of this chapter to view some example analog output applications.

Analog Output Application Examples

NI-DAQmx and all NI ADEs ship with examples you can use to get started with your application.

LabVIEW Example

The following LabVIEW example illustrates a common continuous generation application:

Example Generation Application—Cont Gen Voltage Wfm-Int Clk-Non Regeneration VI located in `labview\examples\DAQmx\Analog Out\Generate Voltage.llb`

LabWindows/CVI Example

The following LabWindows/CVI example in the CVI folder illustrates a common continuous generation application:

Example Generation Application—`samples\DAQmx\Analog Out\Generate Voltage\Cont Gen Volt Wfm-Int Clk`

Synchronization Applications

Note USB devices do *not* support synchronization.

Synchronization Application Overview

Due to the many synchronization configurations possible, there is no way to present a general overview of how to construct a synchronization application. It is important to know the theory behind the configurations, signals involved, and any applicable rules when constructing a synchronization application. Refer to Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about synchronization theory.

Use the synchronization examples to help you get started with your synchronization application. Refer to the *NI-DAQmx Help* or the *LabVIEW Help* for more information about software steps necessary for synchronizing DSA devices.

Synchronization Application Examples

NI-DAQmx and all NI ADEs ship with examples you can use to get started with your application.

The DSA analog input examples support synchronization by including multiple devices in the physical channel string, such as `PXI1Slot2/ai0:7,PXI1Slot3/ai0:7`.

The examples in the `\examples\DAQmx\Synchronization\` directory support synchronization using multiple tasks. Refer to these examples for analog output and multi-rate analog input synchronization examples.

LabVIEW Examples

The following LabVIEW example illustrates synchronized analog input and output applications:

- Example Analog Output Synchronization Application—Multi Device Sync-AI and AO-Shared Timebase & Trig-DSA VI located in `labview\examples\DAQmx\Synchronization\Multi-Device.llb`

LabWindows/CVI Example

The following LabWindows/CVI example in the CVI folder illustrates a synchronized DSA analog input application:

Example Analog Input Application—`samples\DAQmx\Synchronization\Multi-Device\AI-Shared Timebase & Trig-DSA`

A

Device-Specific Information

This appendix contains information about specific National Instruments DSA devices.

Note Refer to `ni.com/manuals` for documentation for devices not listed here.

NI 443*x* Devices

NI 443*x* Features

The NI 443*x* devices are high-performance, high-accuracy analog devices for USB. The NI 4431 device features four analog input channels and one analog output channel. The NI 4432 features five analog input channels. Refer to Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about analog input, analog output, and other feature concepts.

NI 443*x* Analog Input Features

Figure A-1 shows the NI 443*x* analog input circuitry block diagram.

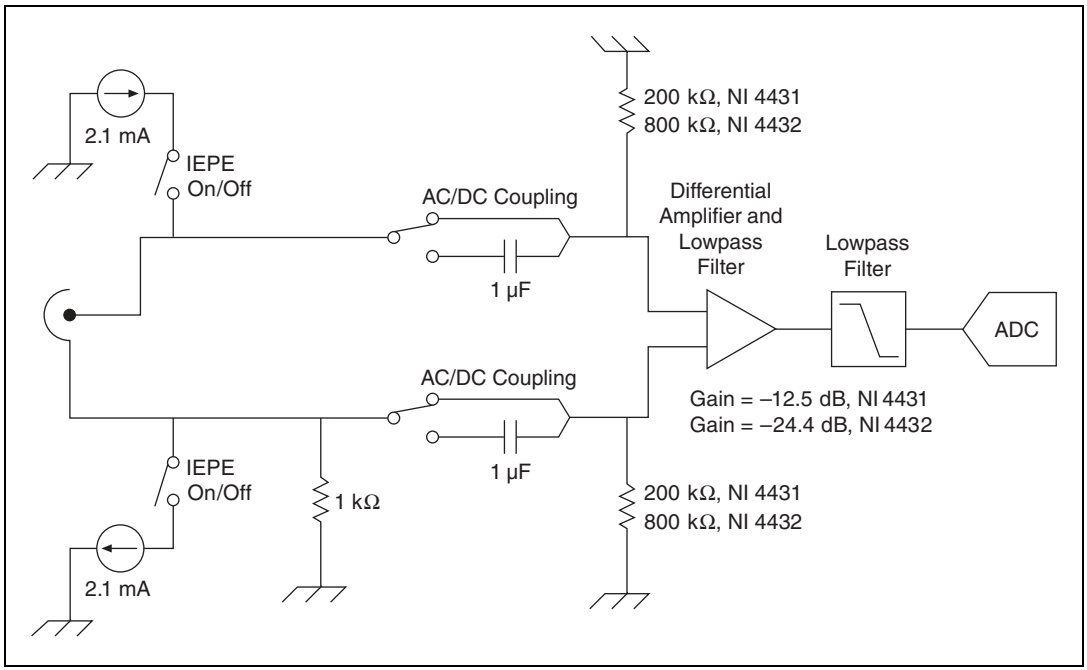

Figure A-1. NI 443*x* Analog Input Block Diagram

The NI 443*x* analog input channels feature the following:

- Sampling rates up to 102.4 kS/s
- Input voltage ranges of either ±10 V_{pk} (NI 4431) to ±40 V_{pk} (NI 4432)
- Per channel AC or DC coupling
- Per channel selectable IEPE current excitation on channels 0..3
- Overload detection
- Anti-alias filtering
- Multiple triggering modes, including external digital triggering

Note When there is no sensor or source connected to a channel configured in DC coupling, it will read approximately 2 V to 2.5 V.

NI 4431 Analog Output Features

Figure A-2 shows the NI 4431 analog output circuitry block diagram.

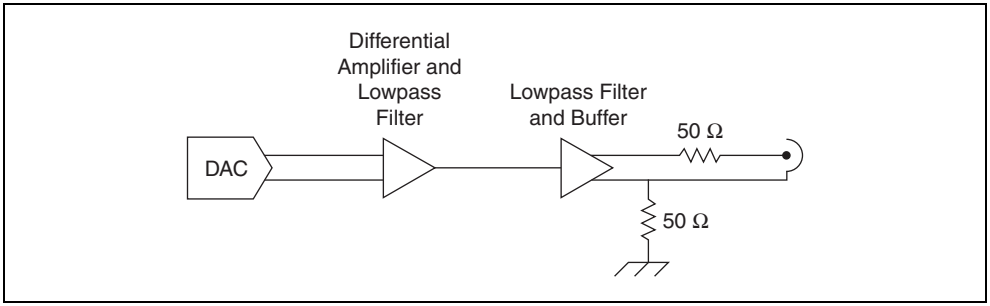

Figure A-2. NI 4431 Analog Output Block Diagram

The NI 4431 analog output channels feature the following:

- Update rates to 96 kS/s
- Output voltage range of ±3.5 V_{pk}
- Anti-image filtering
- External digital triggering
- Onboard waveform regeneration
- Onboard interpolation filtering

NI 443*x* Block Diagrams

NI 4431 Block Diagram

Figure A-3 shows the NI 4431 block diagram.

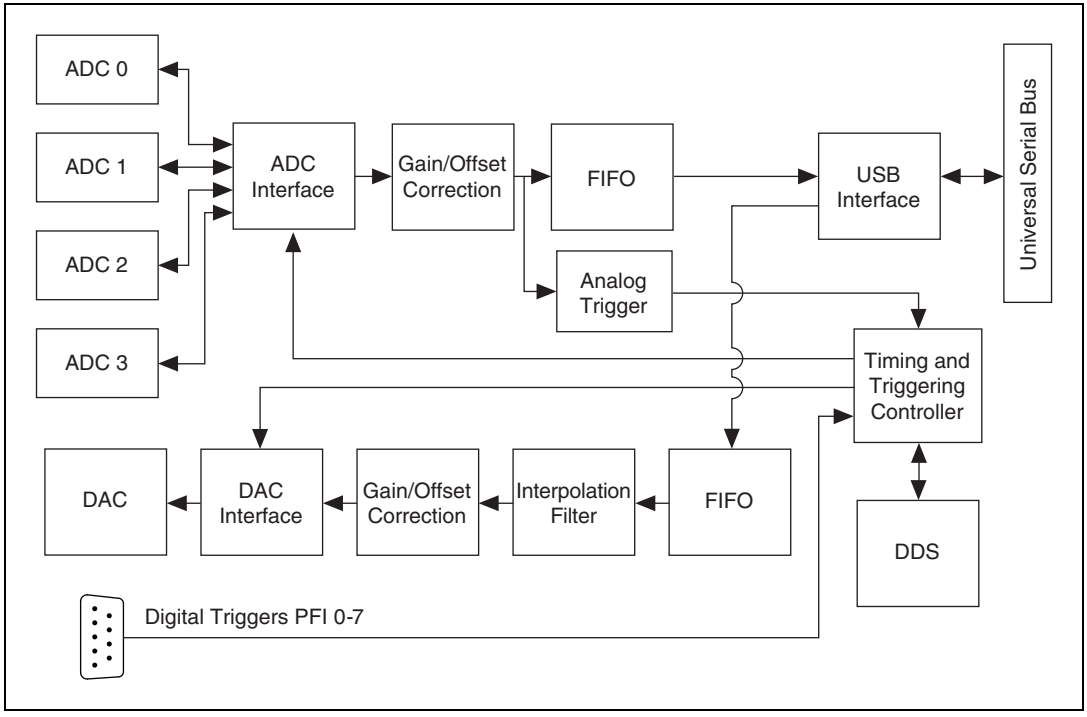

Figure A-3. NI 4431 Block Diagram

NI 4432 Block Diagram

Figure A-4 shows the NI 4432 block diagram.

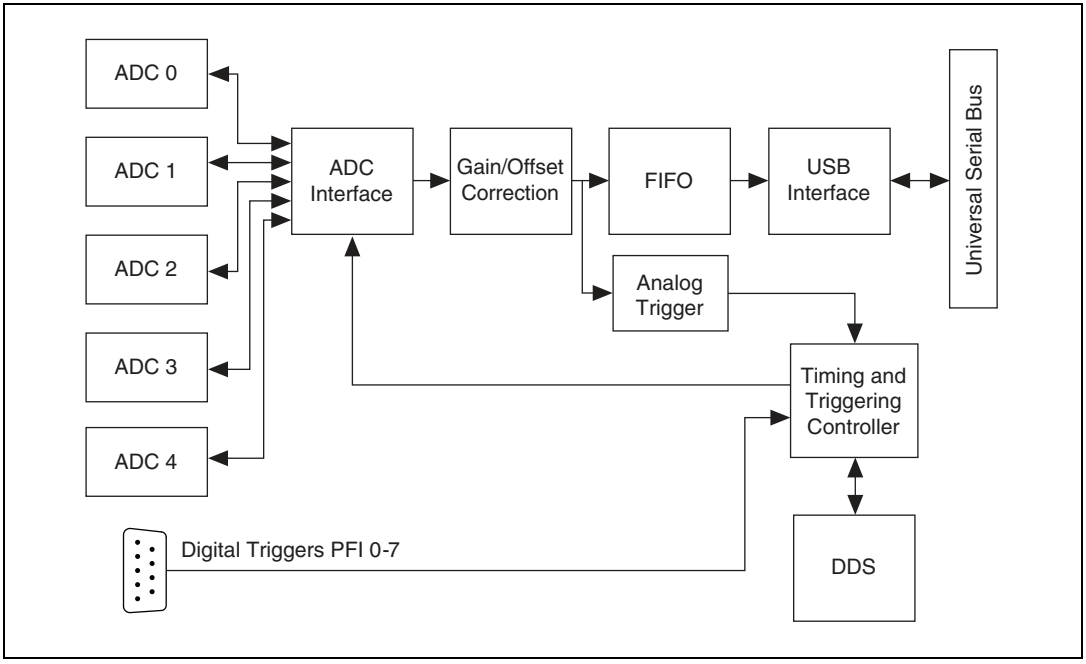

Figure A-4. NI 4432 Block Diagram

Connecting Signals to NI 443*x* Devices

NI 443*x* Front and Rear Panels

Figure A-5 shows the NI USB-4431 and NI USB-4432 front and rear panels. The rear panel is common for both NI 443*x* devices.

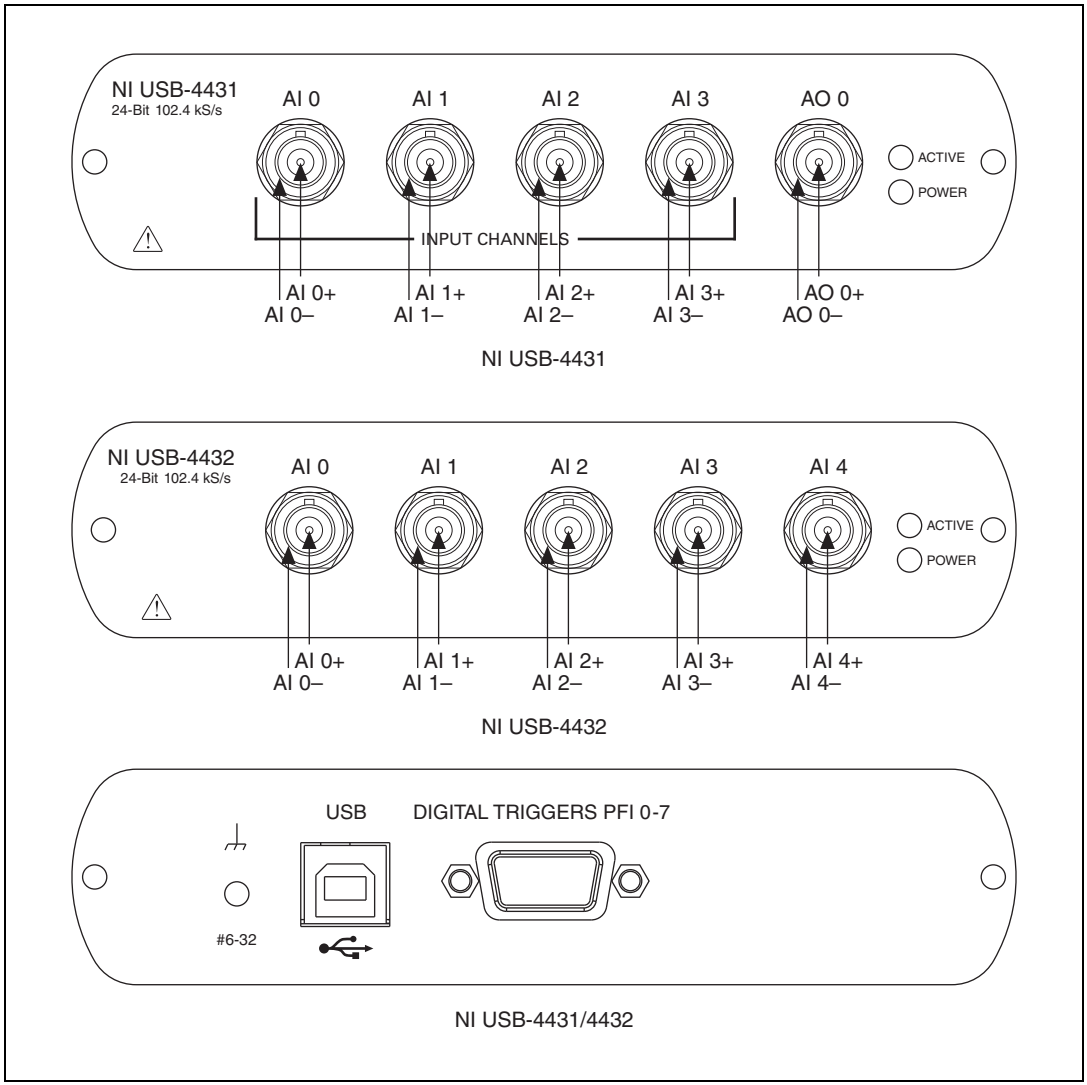

Figure A-5. NI 443*x* Front and Rear Panels

BNC Connector Polarity

Figure A-6 shows the BNC connector polarity for both NI 443*x* devices.

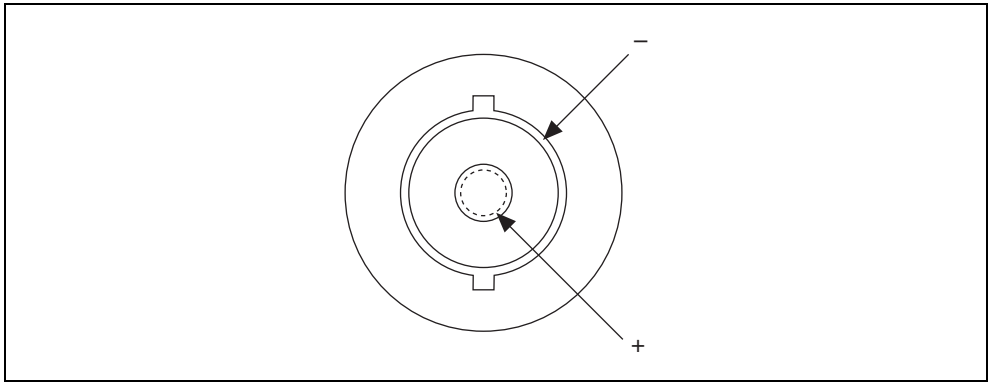

Figure A-6. BNC Connector Polarity for NI 443*x* Devices

NI 443*x* Anti-Aliasing Filter Response

Figure A-7 shows the digital filter input frequency response.

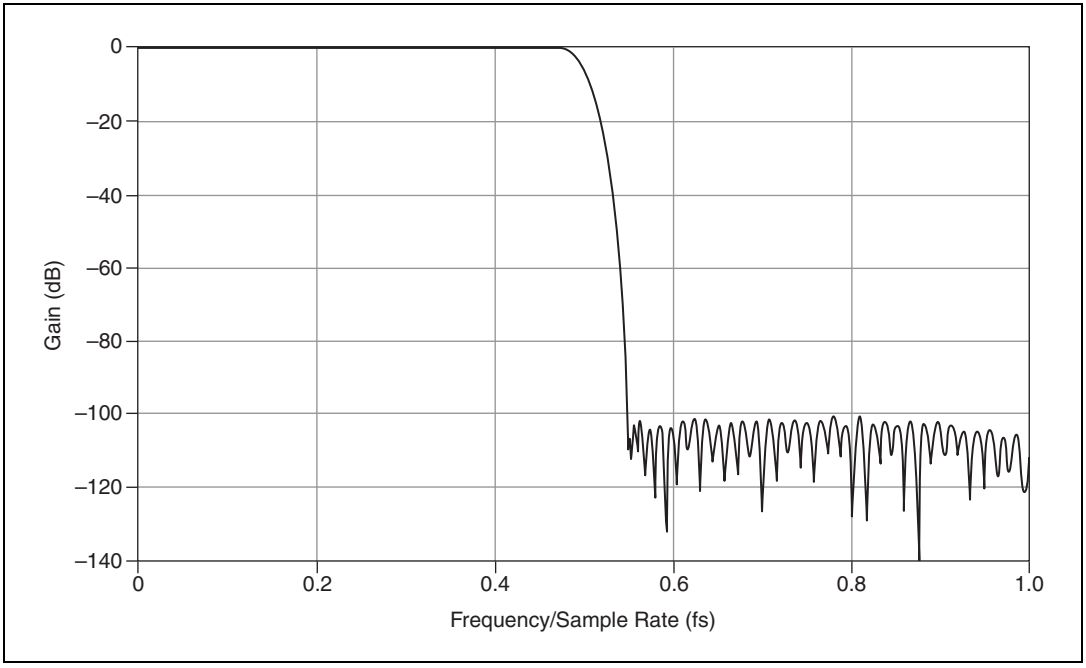

Figure A-7. NI 443*x* Digital Filter Input Frequency Response

Refer to *Analog Output Filters* in Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about the implementation and functionality of the analog and digital anti-aliasing filters.

Figure A-8 and Figure A-9 show the response of the analog input filters. Since the digital filter lets through narrow bands of frequencies at multiples of 64 f_s, it is necessary to use Figure A-7 to know how much attenuation is received by signals in these bands.

For example, when sampling at 51.2 kS/s, the digital filter will remove any out-of-bandwidth tones up until a 51.2 kHz band centered on 64 f_s, or 3.2768 MHz ±25.6 kHz. If noise in the input signal falls into this narrow window, the noise is not rejected by the digital filter. In this limited frequency range, you must consider the analog filter. The analog filter on the NI 4431 has an attenuation of 62 dB at 3.2768 MHz. Therefore, the worst-case alias rejection is 62 dB in this example.

This situation represents the worst-case alias rejections for a sampling rate of 51.2 kS/s. You would only observe this worst-case scenario with a well-defined tone in a narrow frequency range. In real measurement situations, it is more likely that any energy passing the digital filter consists only of low-amplitude noise. If an unwanted component does appear in the digitized signal, increasing the sampling rate might provide an easy solution by both improving the rejection from the analog filter and by repositioning the digital filter so that it can eliminate the alias.

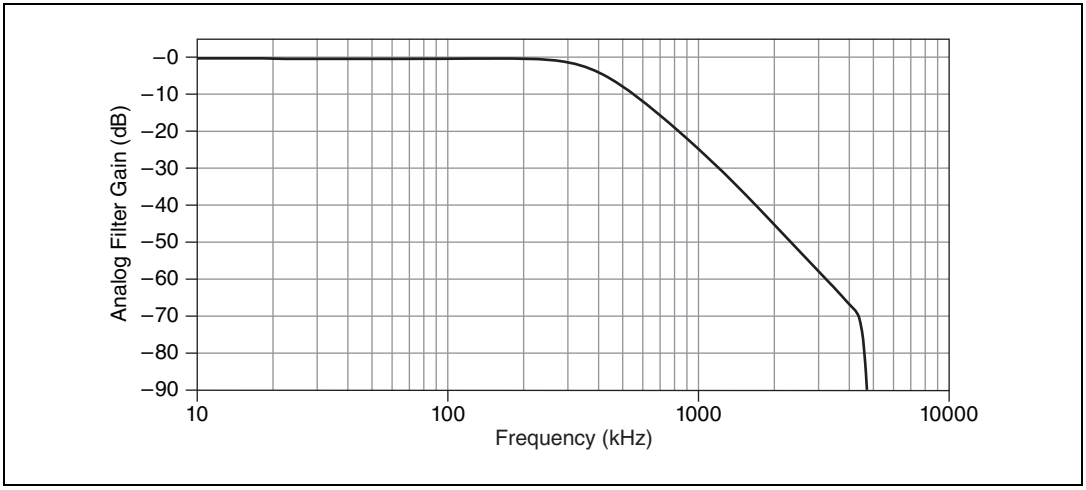

Figure A-8. NI 4431 Analog Filter Response

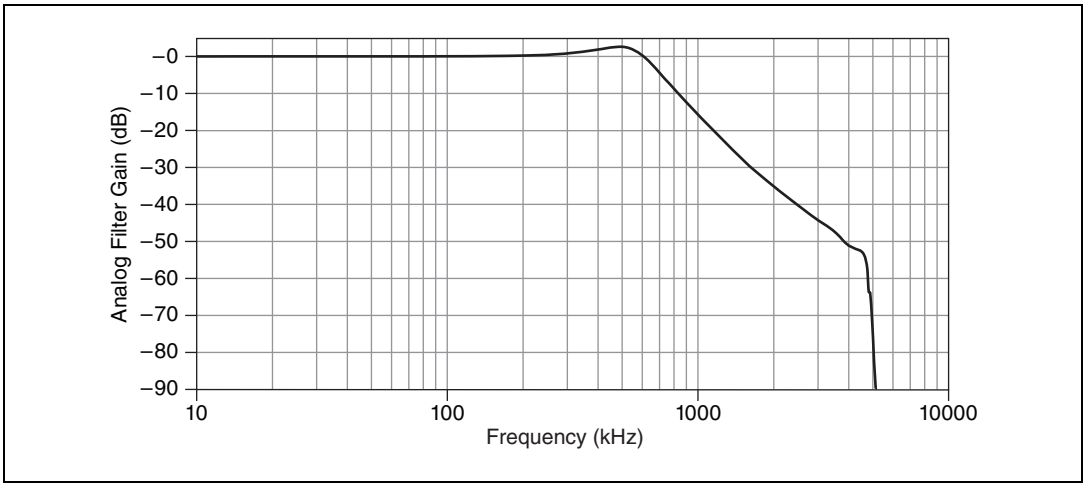

Figure A-9. NI 4432 Analog Filter Response

NI 443*x* Specifications

Refer to the *NI USB-443x Specifications* for more detailed information about the NI 443*x* devices.

NI 446*x* Devices

NI 446*x* Features

The NI 446*x* devices are high-performance, high-accuracy analog devices for PCI and PXI. The NI 4461 devices feature two analog input and two analog output channels with gain and attenuation. The NI 4462 features four analog input channels. Refer to Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about analog input, analog output, gain, attenuation, and other feature concepts.

NI 446*x* Analog Input Features

Figure A-10 shows the NI 446*x* analog input circuitry block diagram.

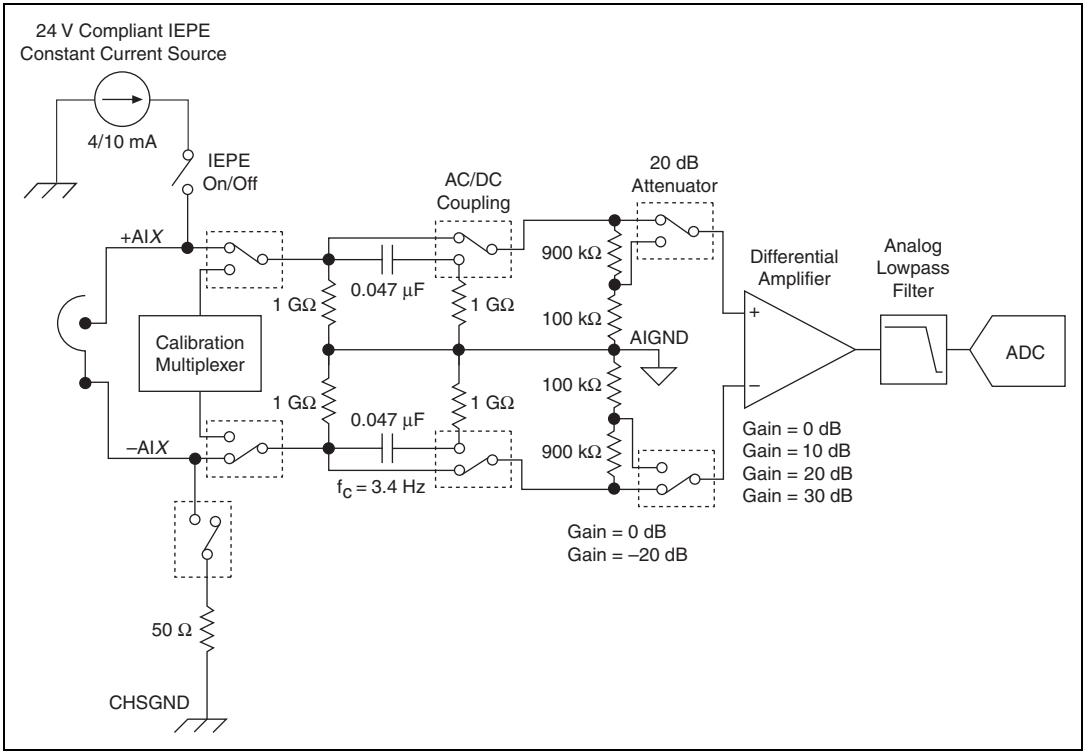

Figure A-10. NI 446*x* Analog Input Block Diagram

The NI 446*x* analog input channels feature the following:

- Sampling rates up to 204.8 kS/s
- Per channel selection of six input voltage ranges from ±0.316 V to ±42.4 V_{pk}
- Per channel differential and pseudodifferential channel configuration
- Per channel AC or DC coupling
- Per channel IEPE current excitation
- Pre-digitization and post-digitization overload detection
- Anti-alias filtering
- Multiple triggering modes, including external digital triggering

NI 4461 Analog Output Features

Figure A-11 shows the NI 4461 analog output circuitry block diagram.

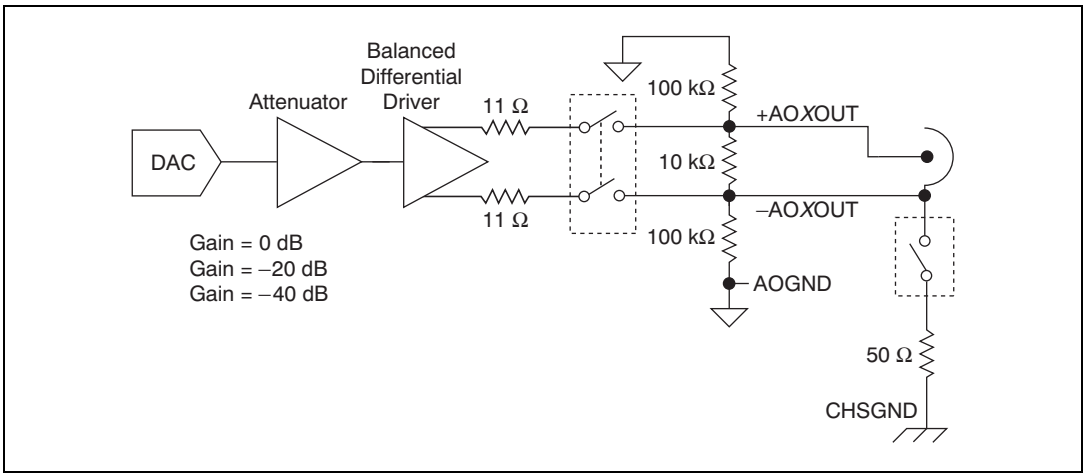

Figure A-11. NI 4461 Analog Output Block Diagram

The NI 4461 analog output channels feature the following:

- Update rates to 204.8 kS/s
- Per channel selection of three output voltages of ±10 V, ±1 V, or ±0.1 V.
- Per channel differential and pseudodifferential channel configuration
- Anti-image filtering
- External digital triggering

NI 446*x* Gain and Attenuation

Positive gain values amplify the signal before the A/D converter (ADC) digitizes it. This signal amplification reduces the measurement range. However, amplifying the signal before digitization allows better resolution by strengthening weak signal components before they reach the ADC. Conversely, negative gains attenuate the signal before they reach the ADC. This attenuation increases the effective measurement range, though it sacrifices dynamic range for weaker signal components. Refer to Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about ADCs.

Note In this manual, AI attenuation is referred to as gain with a negative value. You can set attenuation directly in software by assigning a negative value to the AI.Gain property. Refer to the *NI-DAQmx Help* or the *LabVIEW Help* for more information.

The NI 446*x* has six available gain settings for each AI channel. Each gain setting corresponds to a particular AI range, and each range is centered on 0 V. The gain settings are specified in decibels, where the 0 dB reference is the default input range of ±10 V. Refer to the *NI 446x Specifications* for detailed information about each gain setting and corresponding range.

Caution The range for the −20 dB setting corresponds to a maximum input range of ±42.4 V_{pk}. Setting the gain to −20 dB attenuates the signal by a factor of 10, implying a maximum ADC range of ±100 V. However, the analog front-end circuitry is not rated beyond ±42.4 V_{pk}. When you use this gain setting, the ADC does not saturate at ±42.4 V_{pk}; however, you risk damaging the measurement system or creating a possible safety hazard if you exceed the maximum rated input of ±42.4 V_{pk}.

Table A-1 shows the gain setting sources.

Table A-1. Gain Setting Sources

Gain Setting (dB)	Source
0, 10, 20, 30	Differential amplifier
−10	Combination of −20 and 10 gains
−20	Resistor divider network

In general, select the voltage range that provides the greatest dynamic range and the least distortion. For example, consider an accelerometer with a 100 mV/g sensitivity rating *with a maximum acceleration measurement range of 50 g peak*. This would correspond to a maximum output voltage of 5 V_{pk}. In this case, the ±10 V_{pk} is appropriate, corresponding to 0 dB gain. However, the ±3.16 V_{pk} setting maximizes the dynamic range if you know, for example, that the stimulus is limited to 20 g or 2 V_{pk}.

Minimize system distortion by providing sufficient headroom between the stimulus setting, 2 V_{pk} in this instance, and the range. Choose the next highest range setting above the peak level you expect to measure to provide sufficient headroom. In applications where distortion performance is critical, you can sacrifice overall dynamic range to improve distortion performance by selecting the ±10 V_{pk} setting. Refer to the *NI 446x Specifications* for distortion specifications for each gain setting.

The ADC is the most significant source of measurement noise until you use the 20 dB or 30 dB gain settings. At these higher gain settings, the analog front-end circuitry becomes the dominant noise source. To achieve the best absolute noise performance, select the highest gain setting appropriate for your application.

NI 446*x* Block Diagrams

NI 4461 Block Diagram

Figure A-12 shows the NI 4461 block diagram.

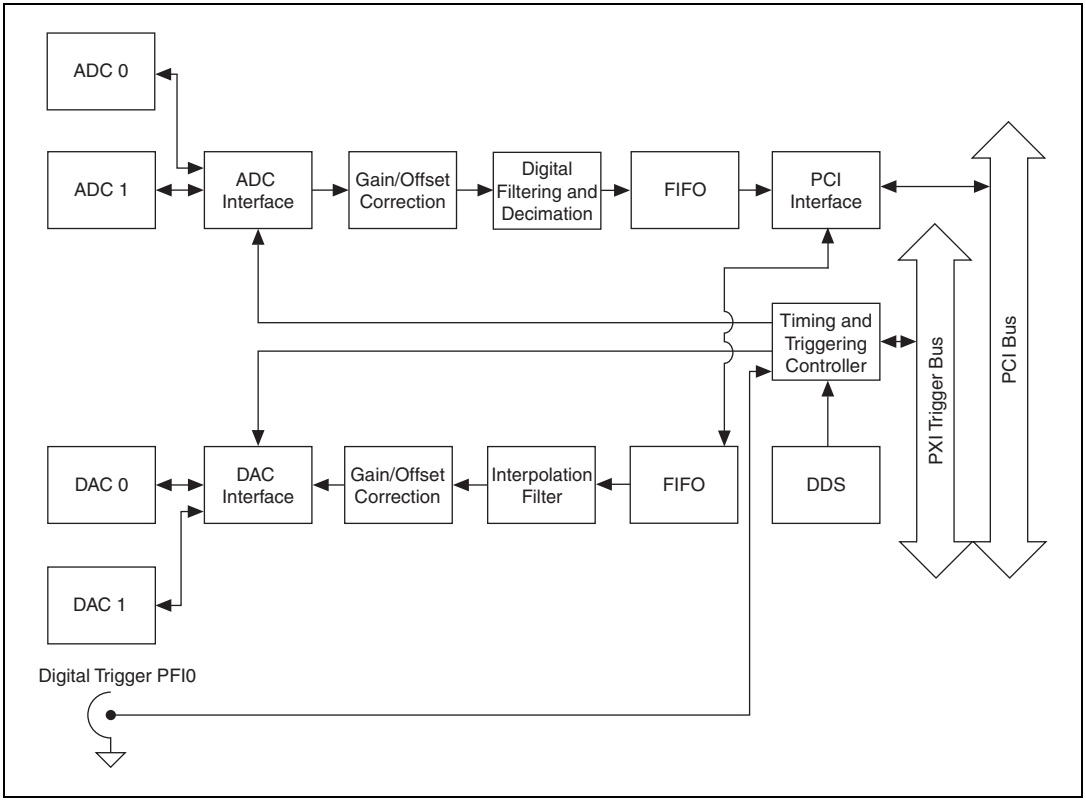

Figure A-12. NI 4461 Block Diagram

NI 4462 Block Diagram

Figure A-13 shows the NI 4462 block diagram.

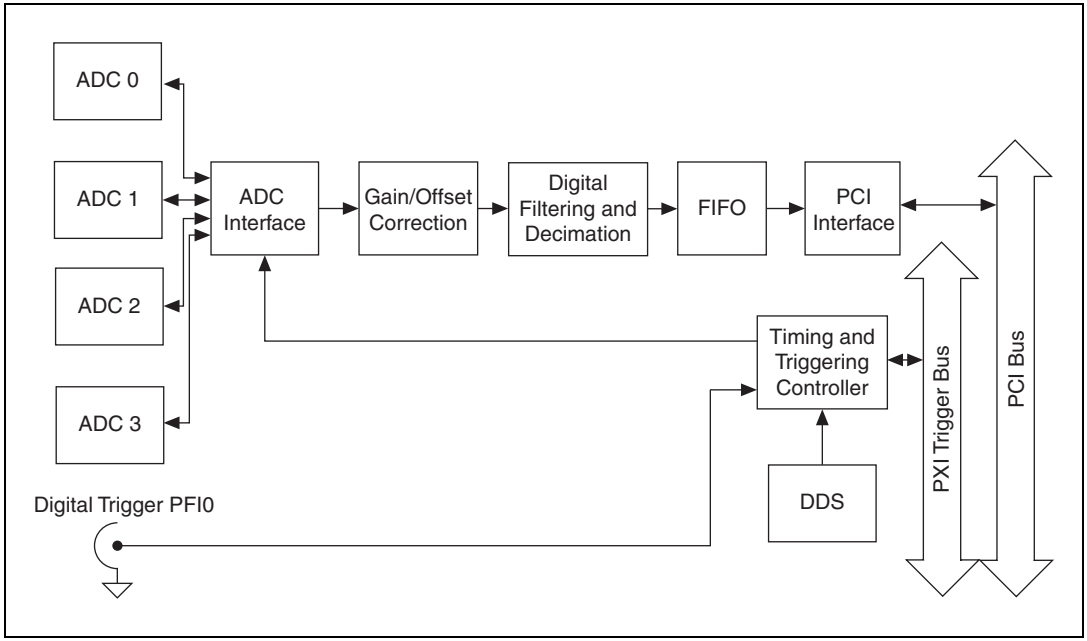

Figure A-13. NI 4462 Block Diagram

Connecting Signals to NI 446*x* Devices

NI 446*x* Front Panels

Figure A-14 shows the NI PXI-4461, NI PCI-4461, NI PXI-4462, and NI PCI-4462 front panels.

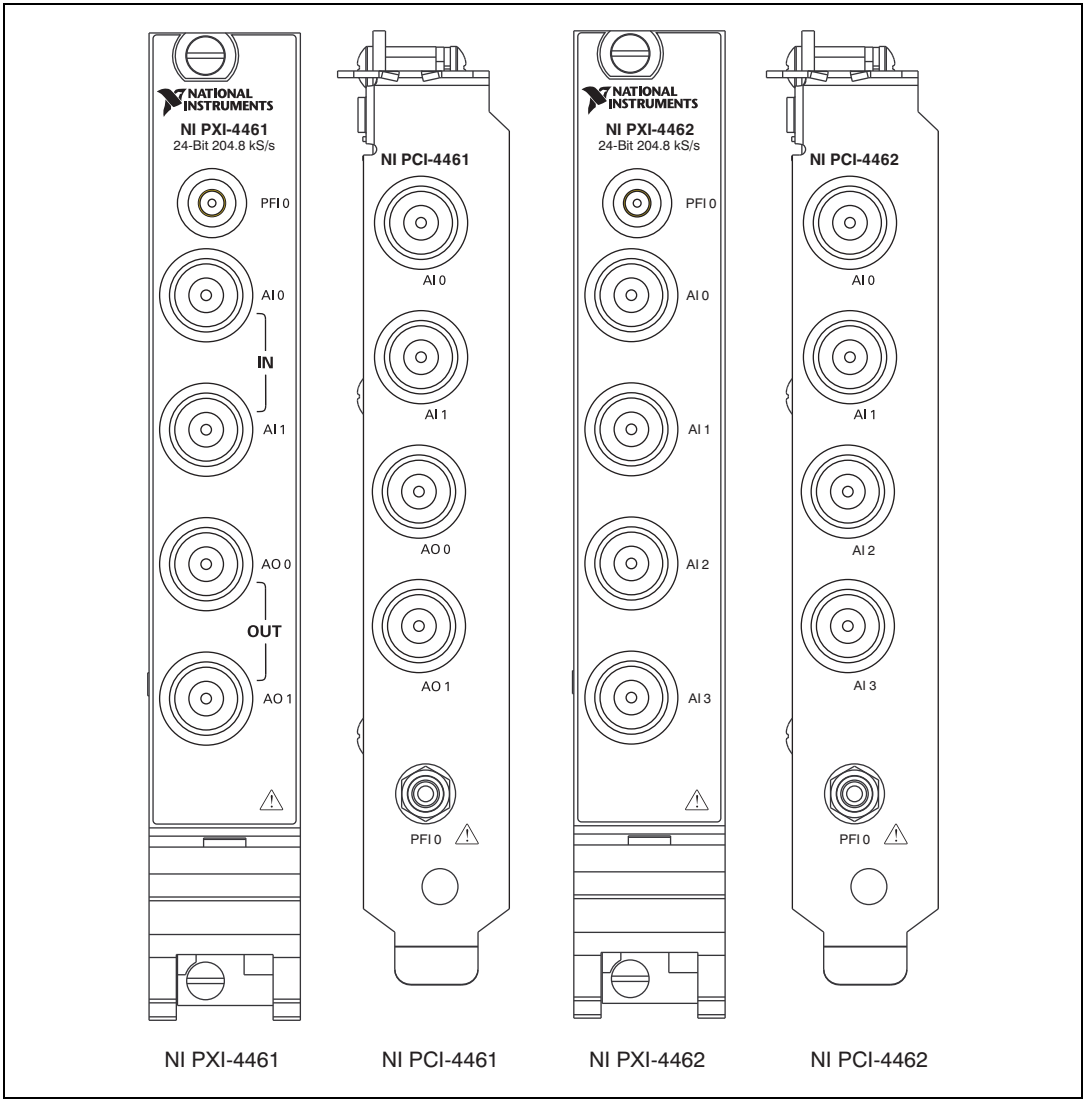

Figure A-14. NI 446*x* Front Panels

BNC Connector Polarity

Figure A-15 shows the BNC connector polarity for all NI 446*x* devices.

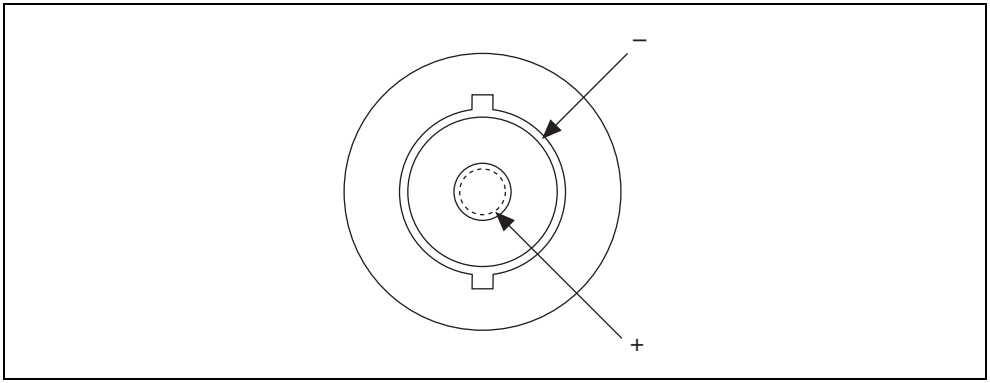

Figure A-15. BNC Connector Polarity for NI 446*x* Devices

NI 446*x* Input Connections

Figure A-16 shows an NI 446*x* input connection with the NI 446*x* terminal configuration in differential mode. Refer to the *Analog Input Channel Configurations* section of Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about terminal configuration.

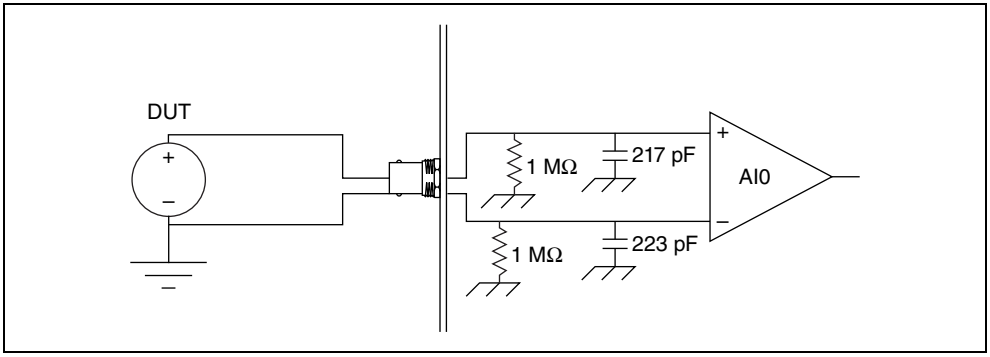

Figure A-16. NI 446*x* Input Connection in Differential Mode

Figure A-17 shows an NI 446*x* input connection with the NI 446*x* terminal configuration in pseudodifferential mode.

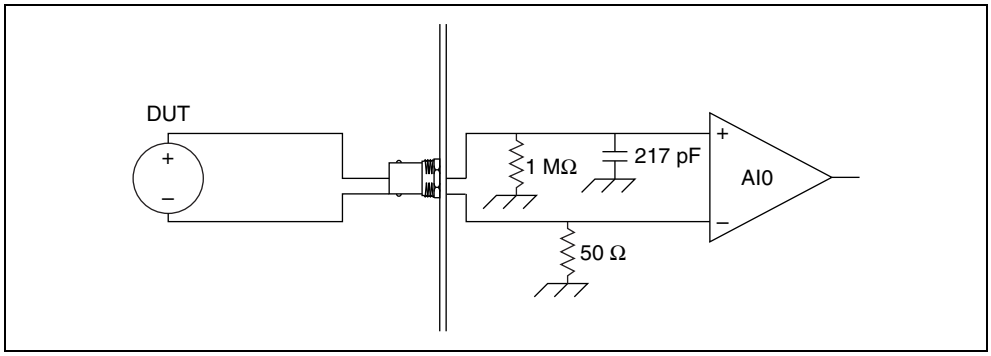

Figure A-17. NI 446*x* Terminal Configuration in Pseudodifferential Mode

NI 4461 Output Connections

Figure A-18 shows an NI 4461 output connection with the NI 4461 terminal configuration in differential mode. Refer to the *Analog Output Channel Configurations* section of Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about terminal configuration.

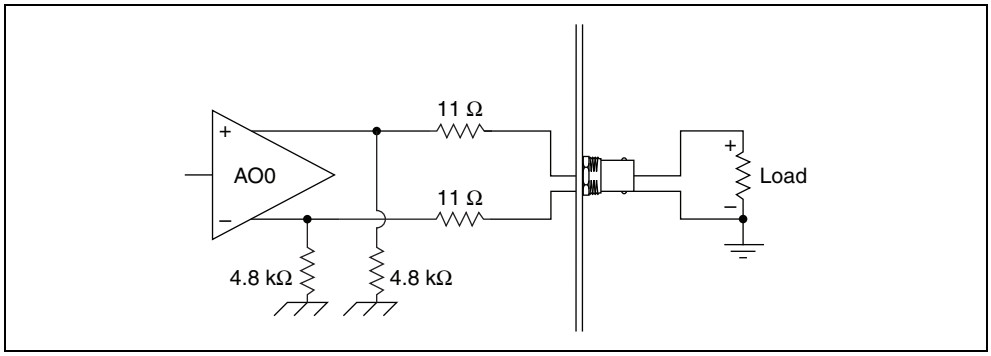

Figure A-18. NI 4461 Output Connection with Terminal Configuration in Differential Mode

Figure A-19 shows an NI 4461 output connection with the NI 4461 terminal configuration in pseudodifferential mode.

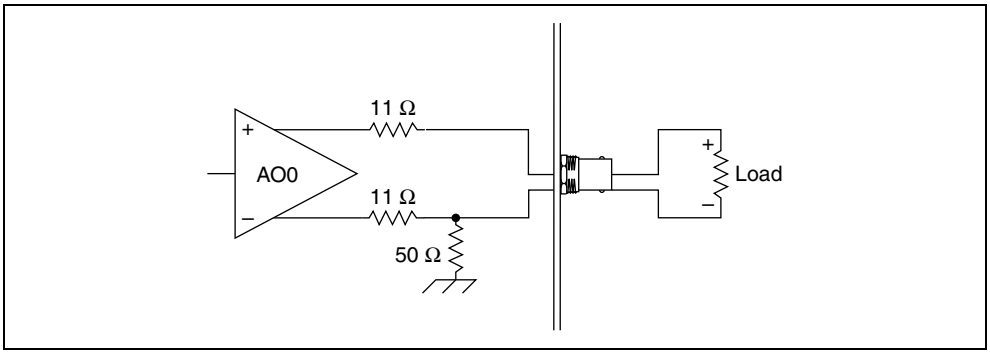

Figure A-19. NI 4461 Output Connection with Terminal Configuration in Pseudodifferential Mode

NI 446*x* Anti-Aliasing Filter Response

Figure A-20 shows the digital filter input frequency response with low-frequency alias rejection enabled.

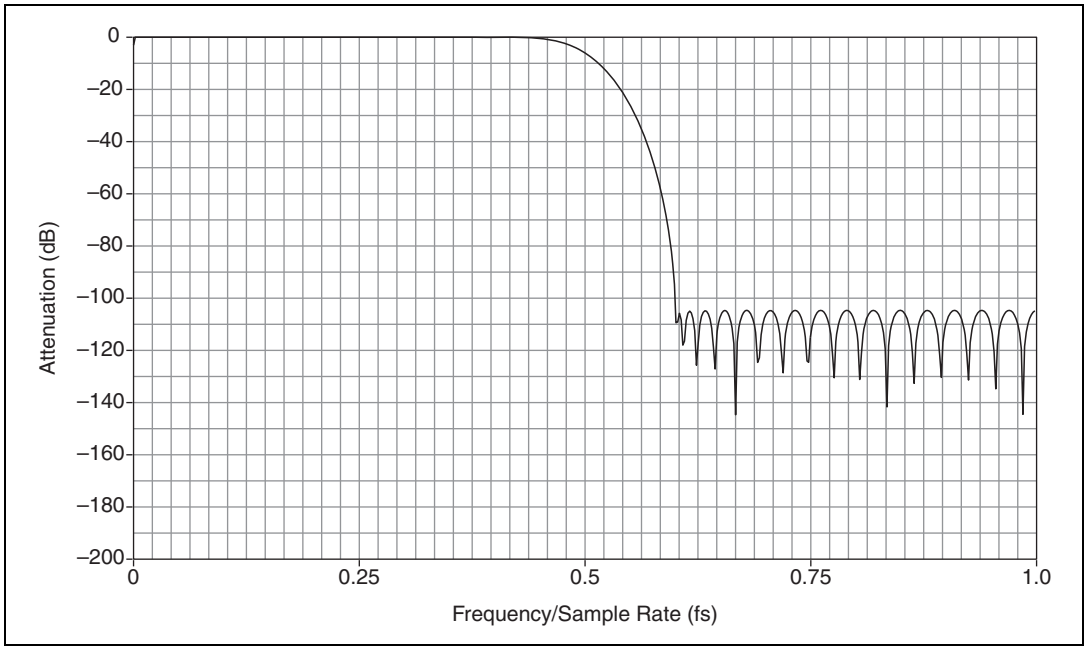

Figure A-20. NI 446*x* Digital Filter Input Frequency Response with Low-Frequency Alias Rejection Enabled

Figure A-21 shows the digital filter input frequency response with low-frequency alias rejection disabled.

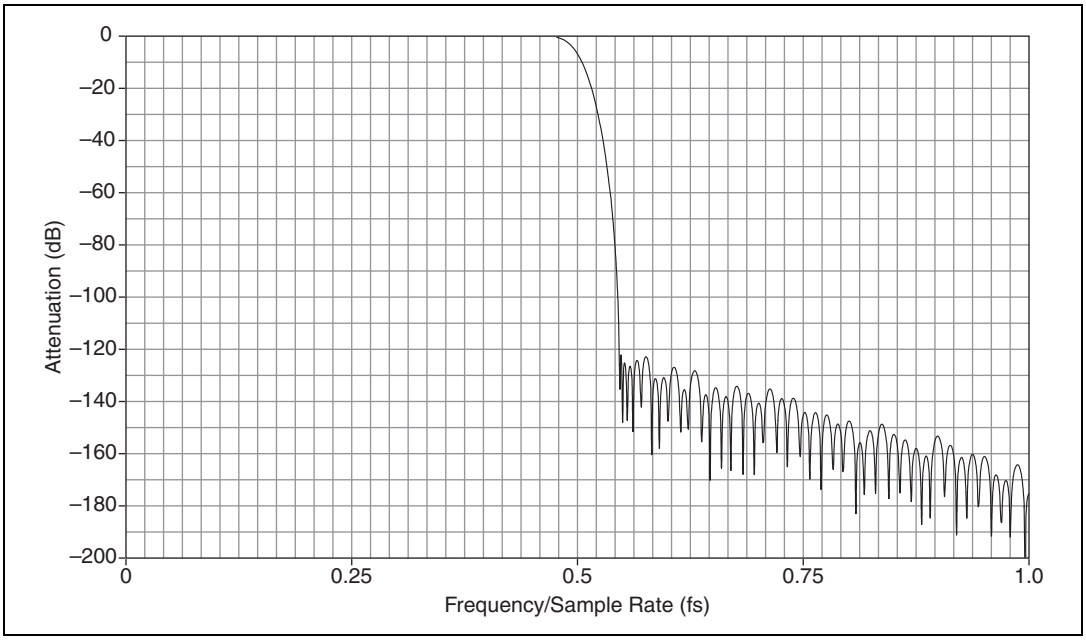

Figure A-21. NI 446*x* Digital Filter Input Frequency Response with Low-Frequency Alias Rejection Disabled

Refer to *Analog Output Filters* in Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about the implementation and functionality of the analog and digital anti-aliasing filters.

Figure A-22 shows the response of the analog anti-aliasing filter with and without enhanced low-frequency alias rejection enabled. Figure A-22 illustrates the alias rejection for a tone that passes the digital filter by falling into one of the f_s-wide bands centered on the oversample rate. The first set of x-axis labels denotes the NI 446*x* sample rate in kS/s. The second set of x-axis labels shows the frequency of an input signal that could pass through the digital filter at the given sampling rate. Refer to the *Anti-Alias Filters* section in Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for information about NI DSA oversample rates. Refer to the *ADC Modulator Oversample Rate* section in the *NI 446x Specifications* for more information.

For example, when sampling at 10 kS/s, the digital filter will remove any out-of-bandwidth tones up to a 10 kHz band centered on 128 f_s, or 1.28 MHz ±5 kHz. If noise in the input signal falls into this narrow window, the noise is not rejected by the digital filter. In this limited frequency range, you must consider the analog filter. Figure A-22 illustrates that with a

sampling rate of 10 kS/s, the analog filter attenuates an input signal frequency of 1.28 MHz by –9 dB without enhanced low-frequency alias rejection enabled. With enhanced low-frequency alias rejection enabled, the attenuation would be –36 dB.

The sawtooth line in Figure A-22 represents the filter response with low-frequency alias rejection enabled. The worst-case alias rejection is approximately –25 dB. This corresponds to the analog filter attenuation at 25.6 kS/s.

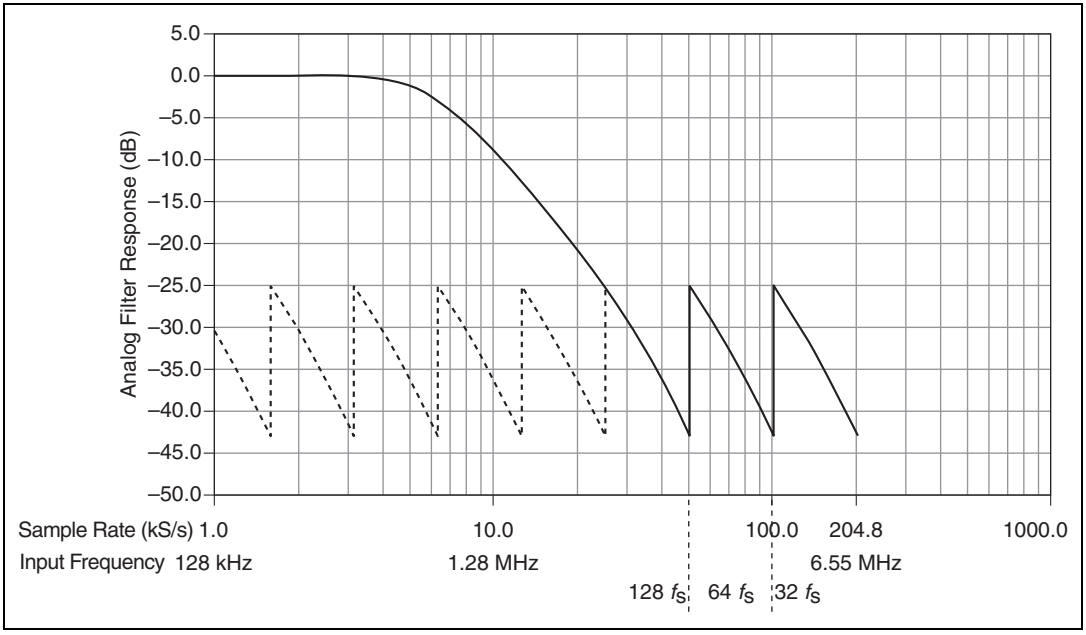

Figure A-22. NI 446*x* Analog Filter Response

This situation represents the worst-case alias rejections for each sampling rate. You would only observe this worst-case scenario with a well-defined tone in a narrow frequency range. In real measurement situations, it is more likely that any energy passing the digital filter consists only of low-amplitude noise. If an unwanted component does appear in the digitized signal, increasing the sampling rate might provide an easy solution by both improving the rejection from the analog filter and by repositioning the digital filter so that it can eliminate the alias.

NI PXI-446*x* Reference Clock Synchronization

NI PXI-446*x* devices employ onboard PLL circuitry. The PLL circuitry locks the onboard 100 MHz voltage-controlled crystal oscillator (VCXO) to the PXI 10 MHz reference clock signal, PXI_CLK10. The VCXO output provides the source for the DDS chip, which generates the sample clock timebase. In this way the NI PXI-446*x* devices lock the sample clock timebase to PXI_CLK10.

NI 446*x* Specifications

Refer to the *NI 446x Specifications* for more detailed information about the NI 446*x* devices.

NI 447*x* Devices

NI 447*x* Features

The NI 447*x* devices are high-performance, high-accuracy analog input devices for PXI and PCI. The NI 4472 features eight input channels. The NI 4472B features eight input channels with a lower cutoff frequency on AC-coupled channels. The NI PCI-4474 features four input channels. Refer to Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about analog input and other feature concepts.

NI 447*x* Analog Input Features

Figure A-23 shows the NI 447*x* analog input circuitry block diagram.

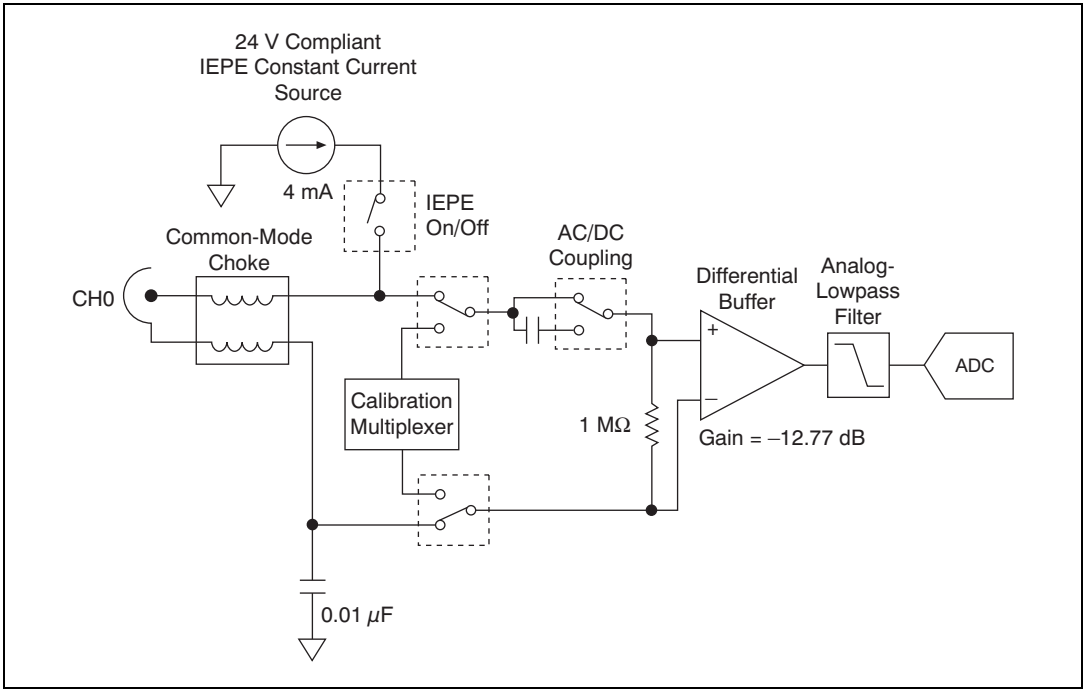

Figure A-23. NI 447*x* Analog Input Block Diagram

The NI 447*x* analog input channels feature the following:

- Simultaneous sampling rates up to 102.4 kS/s
- Per channel AC or DC coupling
- Per channel IEPE current excitation
- Anti-alias filtering
- Postdigitization digital overload detection
- Multiple triggering modes, including external digital triggering

NI 447*x* Block Diagram

Figure A-24 shows the NI 447*x* digital function block diagram.

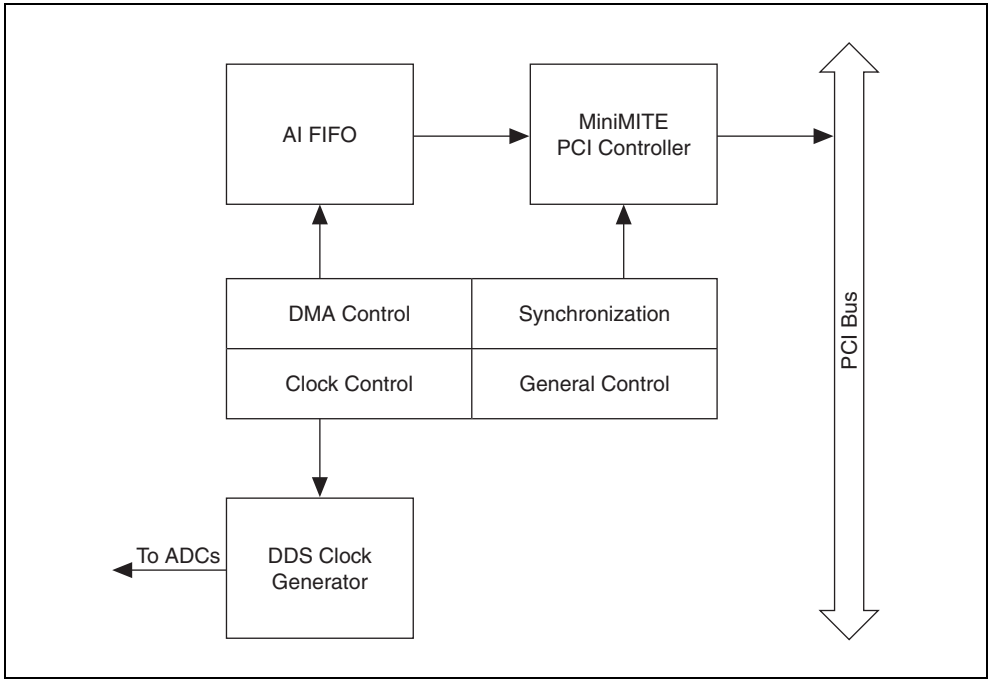

Figure A-24. NI 447*x* Digital Function Block Diagram

Connecting Signals to NI 447*x* Devices

NI 447*x* Front Panels

Figure A-25 shows the NI PXI-4472, NI PXI-4472B, NI PCI-4472, NI PCI-4472B, and NI PCI-4474 front panels.

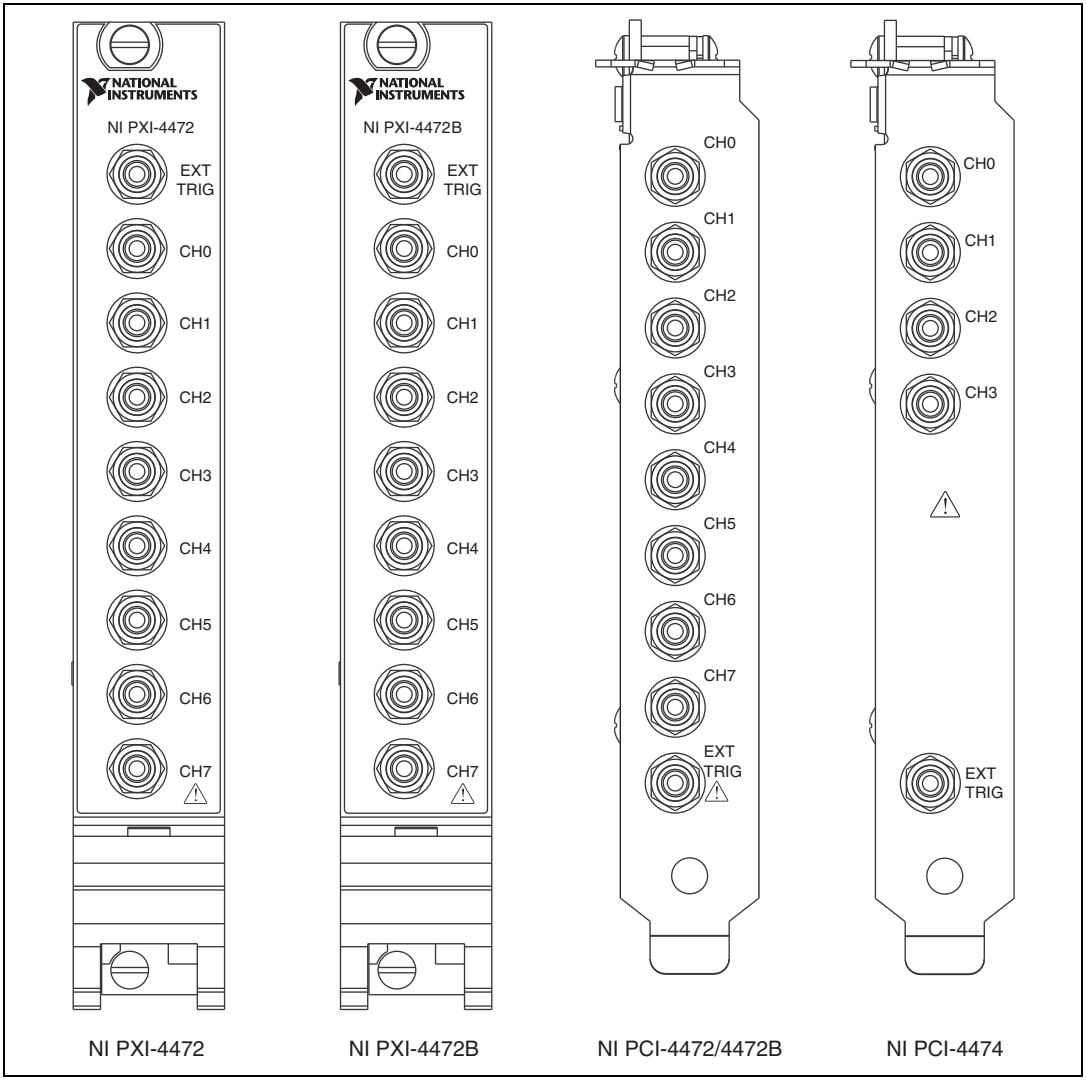

Figure A-25. NI 447*x* Front Panels

NI 447*x* Input Connections

The NI 447*x* channels have pseudodifferential inputs. Figure A-26 shows the *input configurations* for floating and grounded signal sources.

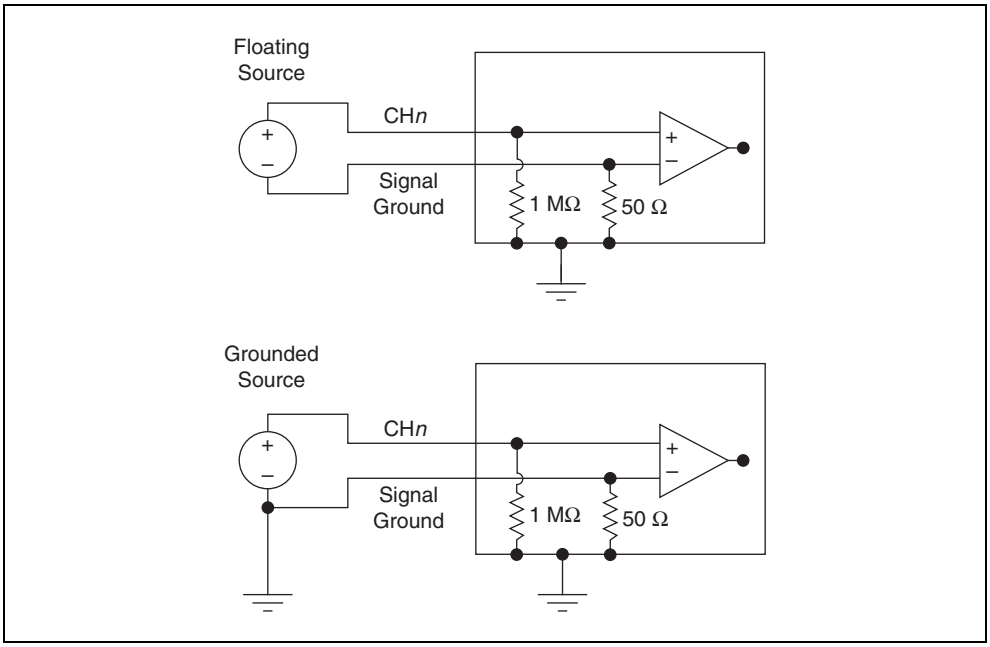

Figure A-26. NI 447*x* Input Connections

Caution Connecting a signal that varies more than ±2.5 V from the NI 447*x* ground reference to the ground (shield) of any input channel can result in inaccurate measurements or damage to the device. NI is *not* responsible for damage caused by such connections.

NI 447*x* Anti-Aliasing Filter Response

Figure A-27 shows the digital filter input frequency response.

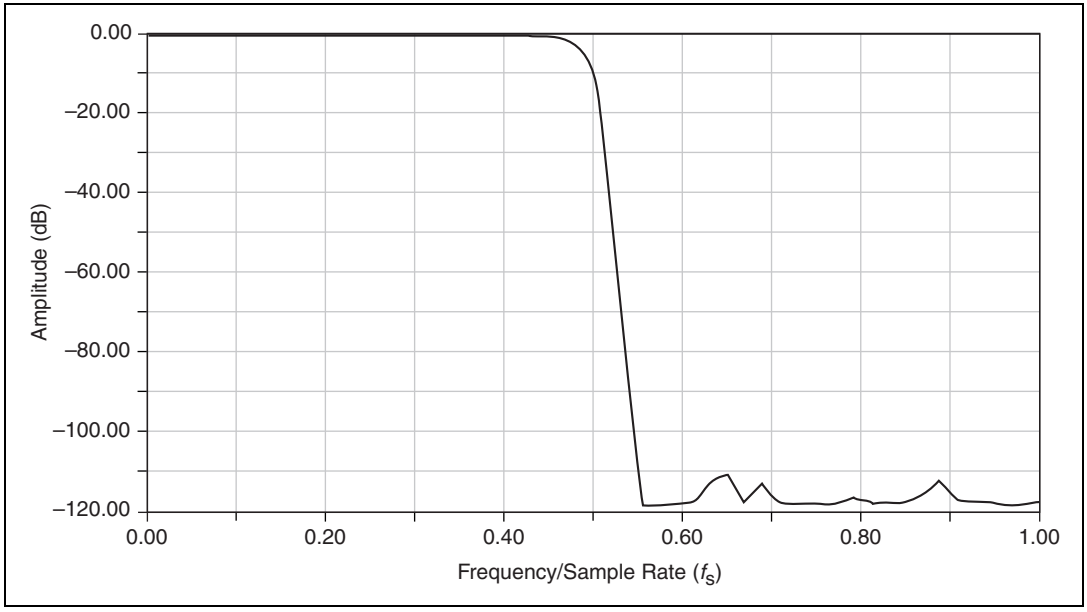

Figure A-27. NI 447*x* Digital Filter Input Frequency Response

Figure A-28 shows the digital filter frequency response near the cut-off point.

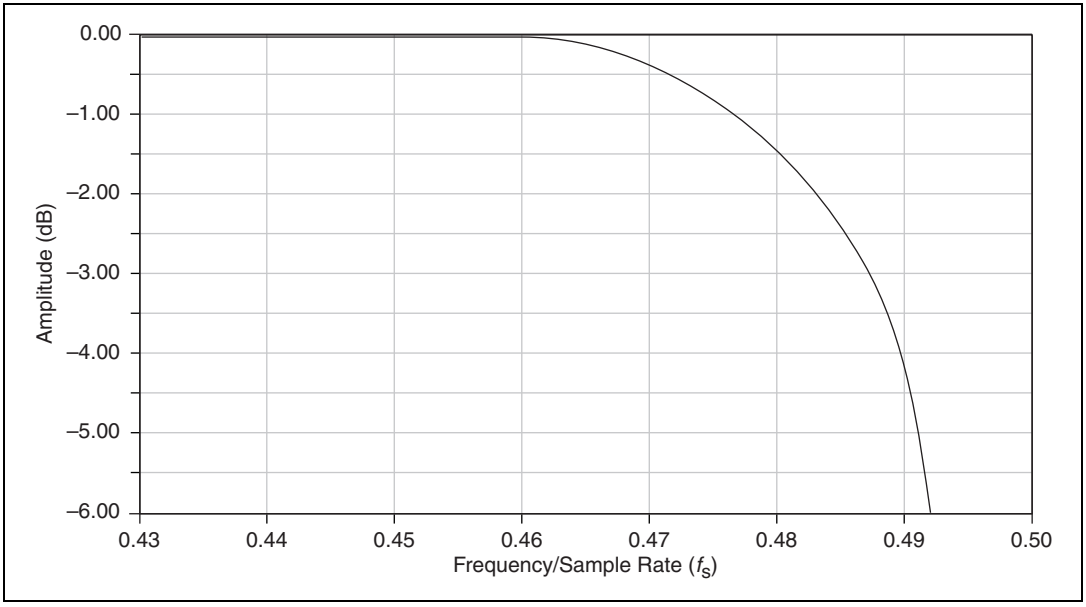

Figure A-28. NI 447*x* Digital Filter Frequency Response Near the Cut-off Point

Refer to *Analog Output Filters* in Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about the implementation and functionality of the analog and digital anti-aliasing filters.

Figure A-29 shows the response of the analog anti-aliasing filter with and without enhanced low-frequency alias rejection enabled. Figure A-29 illustrates the alias rejection for a tone that passes the digital filter by falling into one of the f_s-wide bands centered on the oversample rate. The first set of x-axis labels denotes the NI 447*x* sample rate in kS/s. The second set of x-axis labels shows the frequency of an input signal that could pass through the digital filter at the given sampling rate. Refer to the *Anti-Alias Filters* section in Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for information about NI DSA oversample rates. Refer to the *ADC Modulator Oversample Rate* section in the *NI 447x Specifications* for more information.

For example, when sampling at 10 kS/s, the digital filter will remove any out-of-bandwidth tones up to a 10 kHz band centered on 128 f_s, or 1.28 MHz ±5 kHz. If noise in the input signal falls into this narrow window, the noise is not rejected by the digital filter. In this limited frequency range, you must consider the analog filter. Figure A-29 illustrates that with a sampling rate of 10 kS/s, the analog filter attenuates an input signal frequency of 1.28 MHz by –37 dB without enhanced low-frequency alias rejection enabled. With enhanced low-frequency alias rejection enabled, the attenuation would be –80 dB.

The sawtooth line in Figure A-29 represents the filter response with low-frequency alias rejection enabled. The worst-case alias rejection is approximately –63 dB. This corresponds to the analog filter attenuation at 25.6 kS/s.

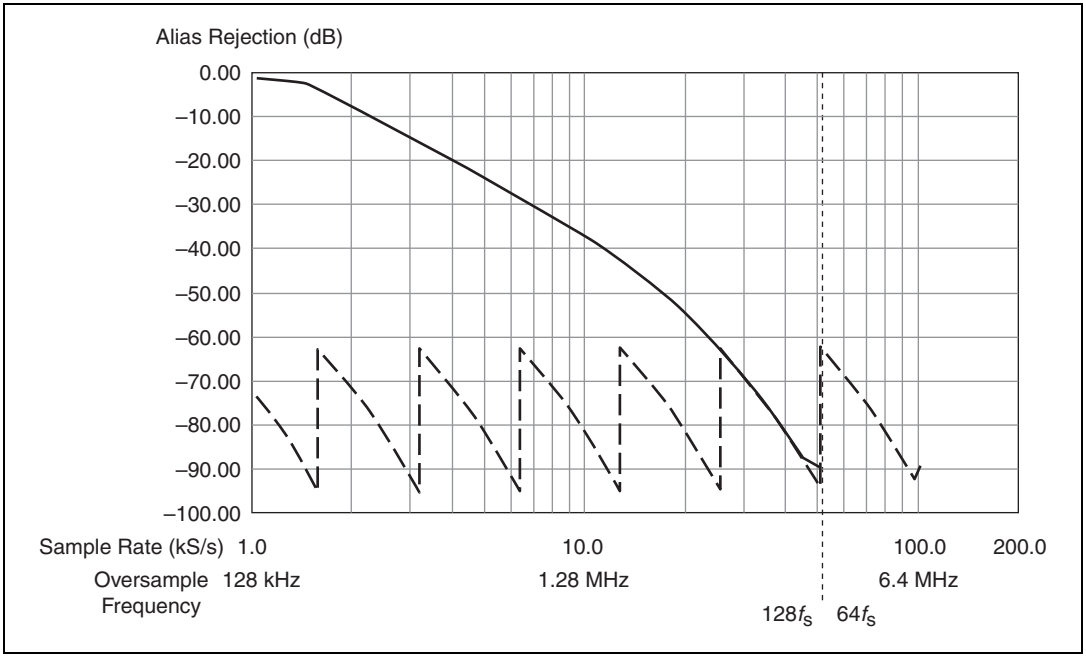

Figure A-29. NI 447*x* Analog Filter Response

This situation represents the set of worst-case alias rejections for each sample rate. You would only observe this worst-case scenario with a well-defined tone in a narrow frequency range. In real measurement situations, it is more likely that any energy passing the digital filter consists only of low-amplitude noise. If an unwanted component does appear in the digitized signal, increasing the sampling rate might provide an easy solution by both improving the rejection from the analog filter and by repositioning the digital filter so that it can eliminate the alias.

NI 447*x* Specifications

Refer to the *NI 447x Specifications* for more detailed information about the NI 447*x* devices.

NI 449*x* Devices

NI 449*x* Features

The NI 449*x* devices are high-performance, high-accuracy analog input devices for PXI or PXIe.

Table A-2 shows different features across the NI 449*x* product line. Refer to Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about analog input and other feature concepts.

Table A-2. NI 449*x* features

Device	Coupling	Gain (dB)	Channels	IEPE	TEDS
NI 4499	AC/DC selectable	0, 10, 20, 30	16	Yes	Yes
NI 4498	AC only	0, 10, 20, 30	16	Yes	Yes
NI 4497	AC/DC selectable	0, 20	16	Yes	Yes
NI 4496	AC only	0, 20	16	Yes	Yes
NI 4495	DC only	0, 20	16	No	No
NI 4492	AC/DC selectable	0, 20	8	Yes	Yes

NI 449*x* Analog Input Features

Figure A-30 shows the NI 4499, NI 4497, and NI 4492 analog input circuitry block diagram.

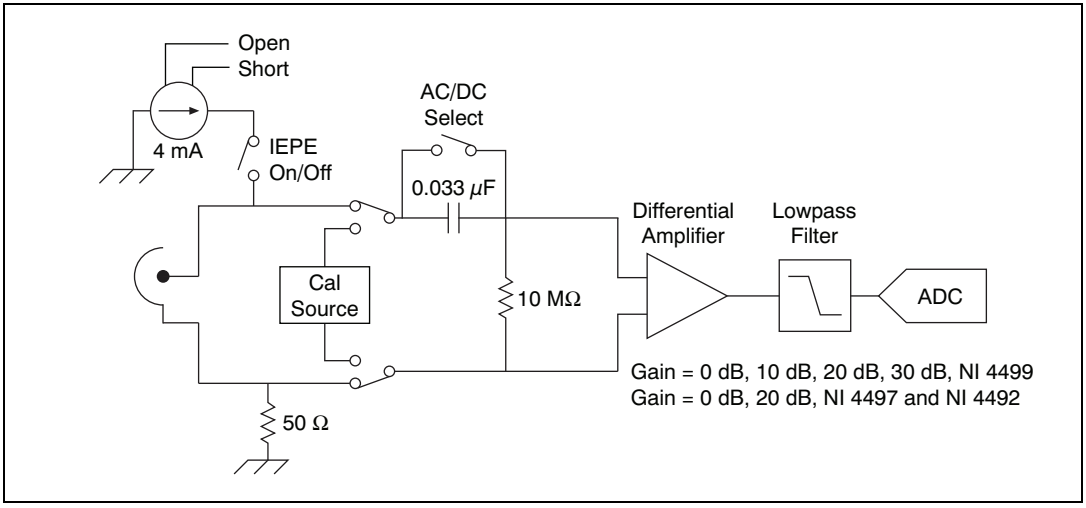

Figure A-30. NI 4499, NI 4497, and NI 4492 Analog Input Block Diagram

Figure A-31 shows the NI 4498 and NI 4496 analog input circuitry block diagram.

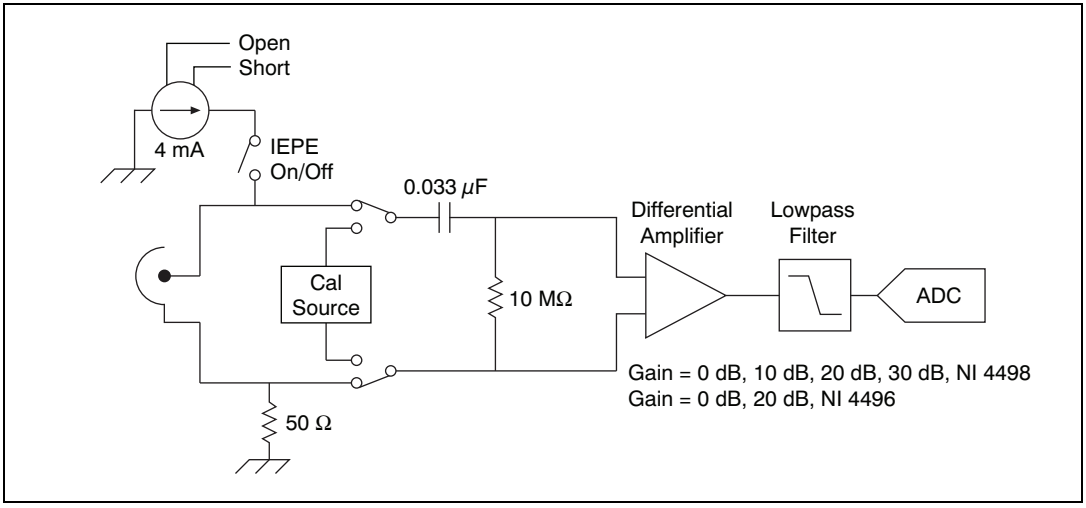

Figure A-31. NI 4498 and NI 4496 Analog Input Block Diagram

Figure A-32 shows the NI 4495 analog input circuitry block diagram.

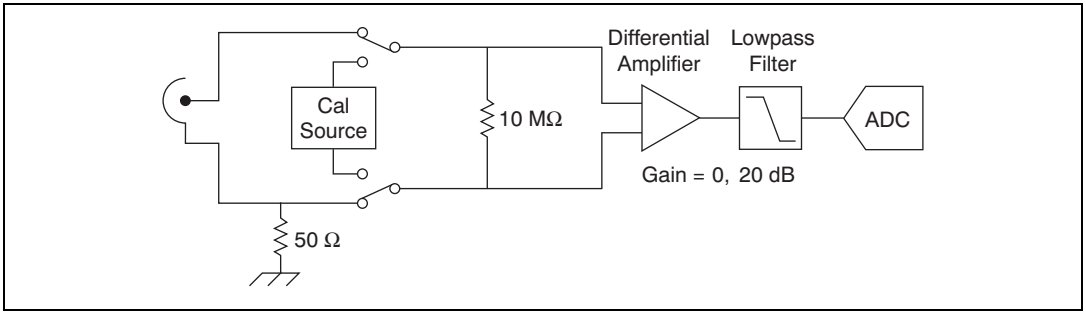

Figure A-32. NI 4495 Analog Input Block Diagram

Note Certain NI 449*x* devices support different gain options. Refer to the *NI 449x Specifications* for more information about supported gain settings.

The NI 449*x* analog input channels feature the following:

- Simultaneous sampling rates up to 204.8 kS/s
- Per channel selection of gain
- Per channel IEPE current excitation (all models except the NI 4495)
- Per channel IEPE sensor open and short detect (all models except the NI 4495)
- Multiple triggering modes, including external digital triggering
- Per channel digital overload detection
- Hardware data packing
- TEDS (NI 4499, NI 4498, NI 4497, NI 4496, NI 4492)

NI 449*x* Block Diagram

Figure A-33 shows the NI 449*x* block diagram.

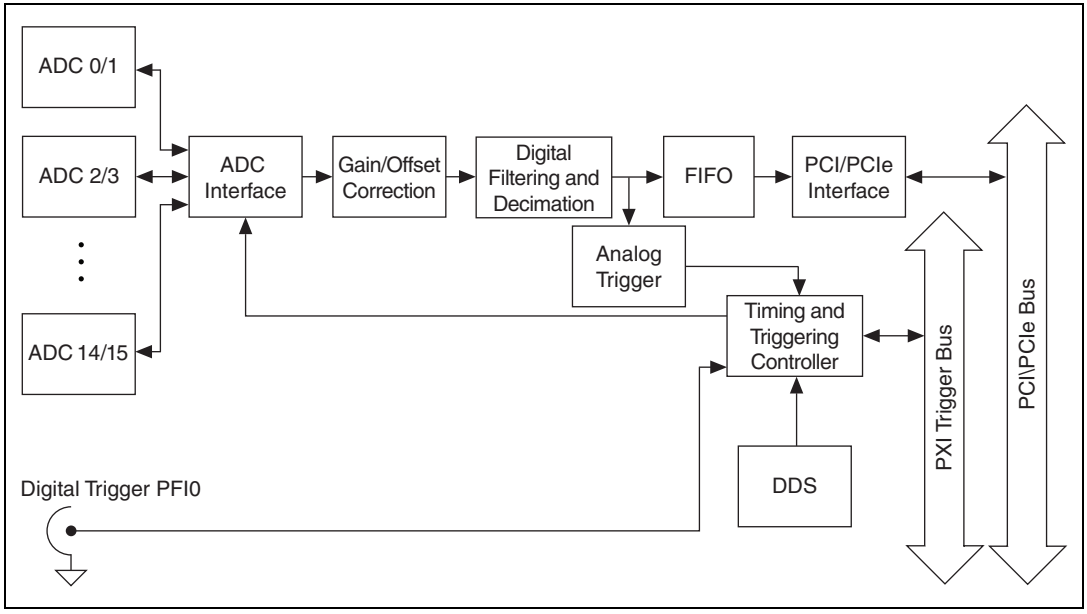

Figure A-33. NI 449*x* Block Diagram

Connecting Signals to NI 449*x* Devices

NI 449*x* Front Panels

Figure A-34 shows the NI 4498, NI 4496, and NI 4495 front panels. Figure A-35 shows the NI 4499, NI 4497, and NI 4492 front panels. The NI 449*x* devices have InfiniBand 4x connectors. Refer to the *NI-DAQmx Help* for more information about the NI 449*x* connectors.

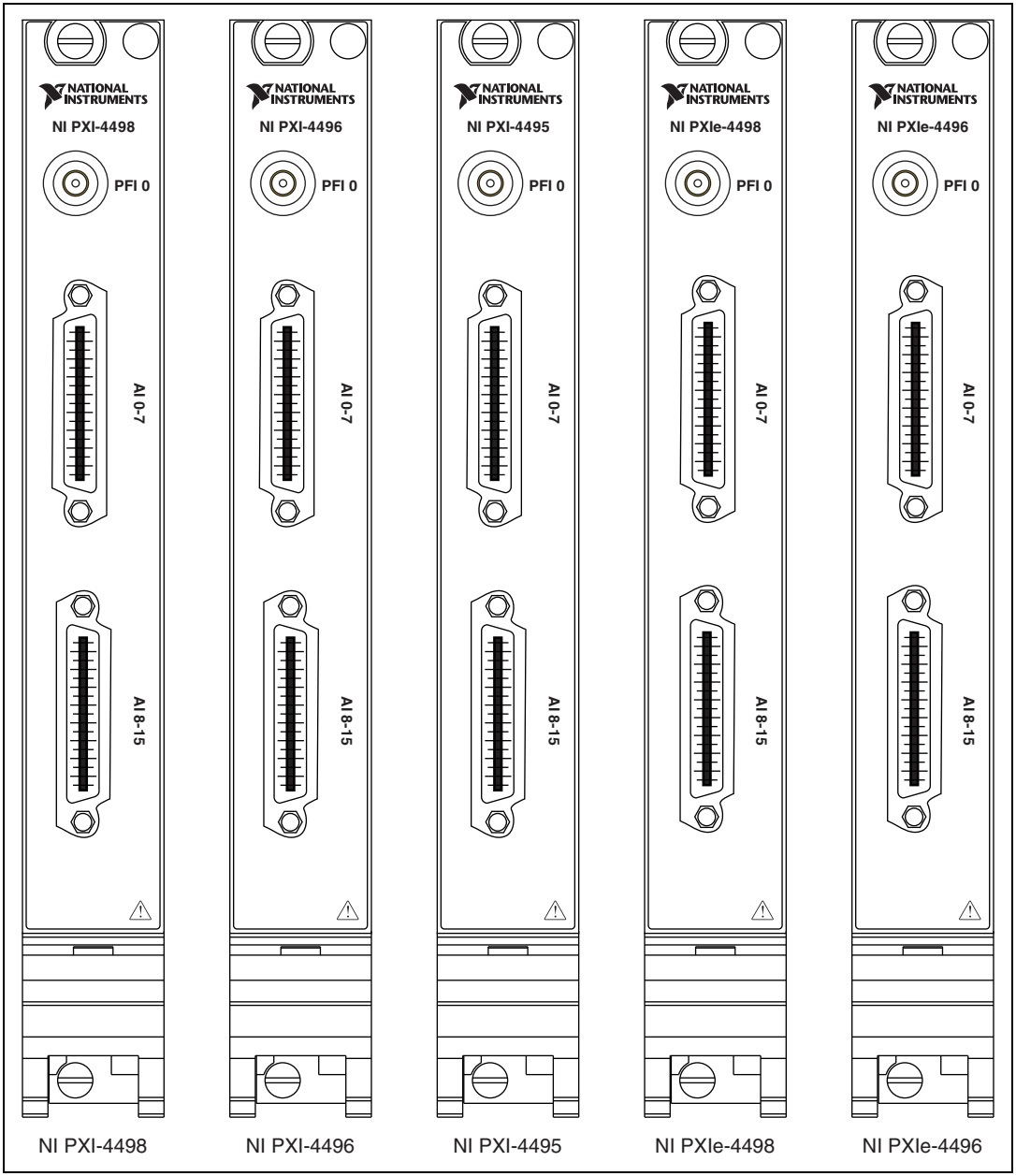

Figure A-34. NI 4498/4496/4495 Front Panels

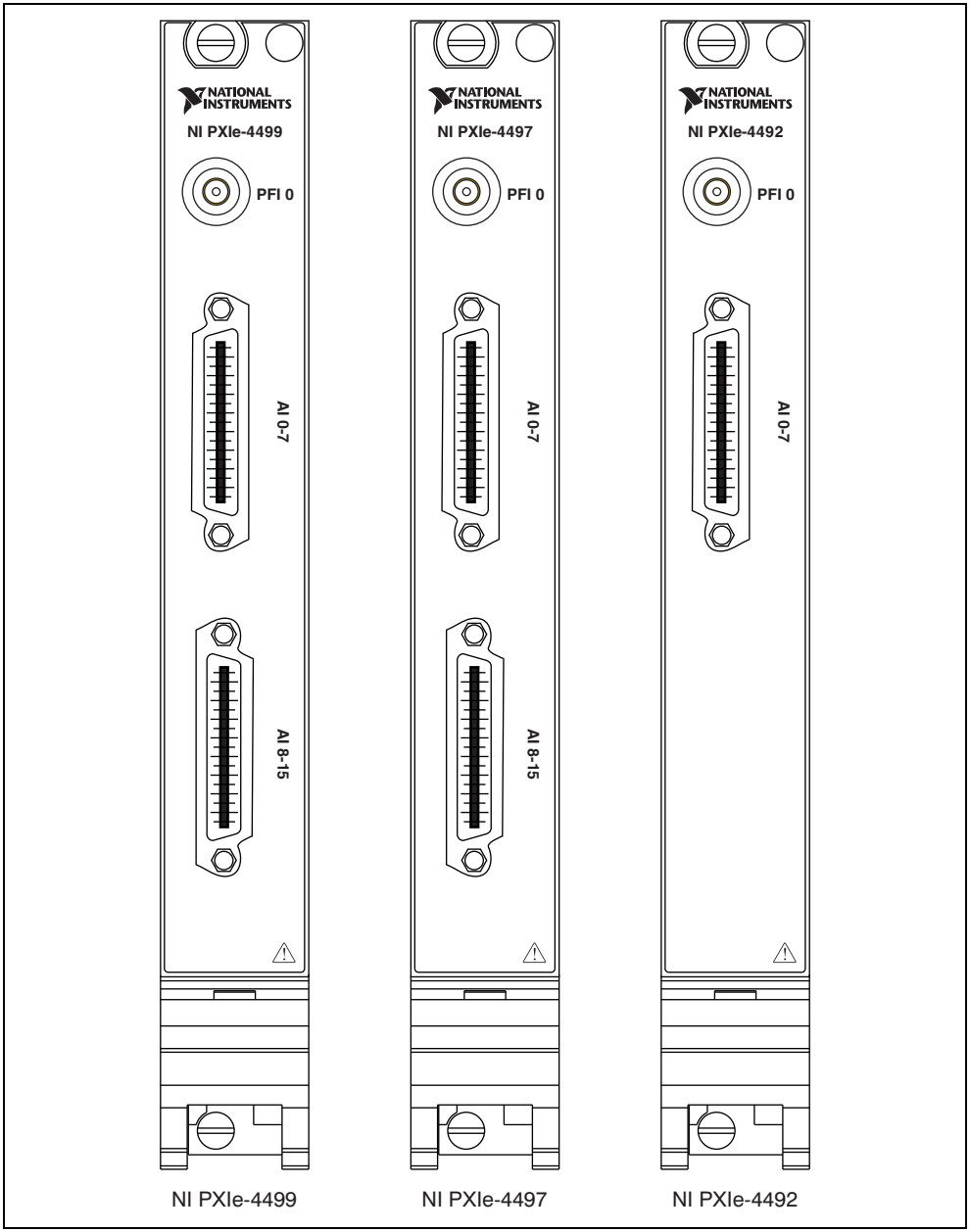

Figure A-35. NI 4499/4497/4492 Front Panels

Caution Connecting a signal that varies more than ±5 V from the NI 449*x* ground reference to the ground (shield) of any input channel can result in damage to the device. NI is *not* responsible for damage caused by such connections.

BNC Connector Polarity

You can use an NI BNC-2144 or an Infiniband 4x to 8 BNC cable assembly to create BNC connectors from the NI 449*x*. Figure A-36 shows the BNC connector polarity for all NI 449*x* devices.

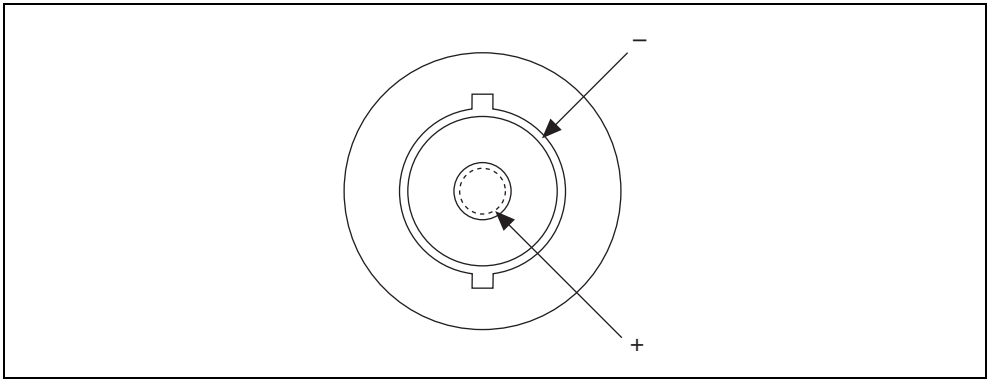

Figure A-36. BNC Connector Polarity for NI 449*x* Devices

NI 449*x* Anti-Aliasing Filter Response

Figure A-37 shows the digital filter input frequency response with low-frequency alias rejection enabled.

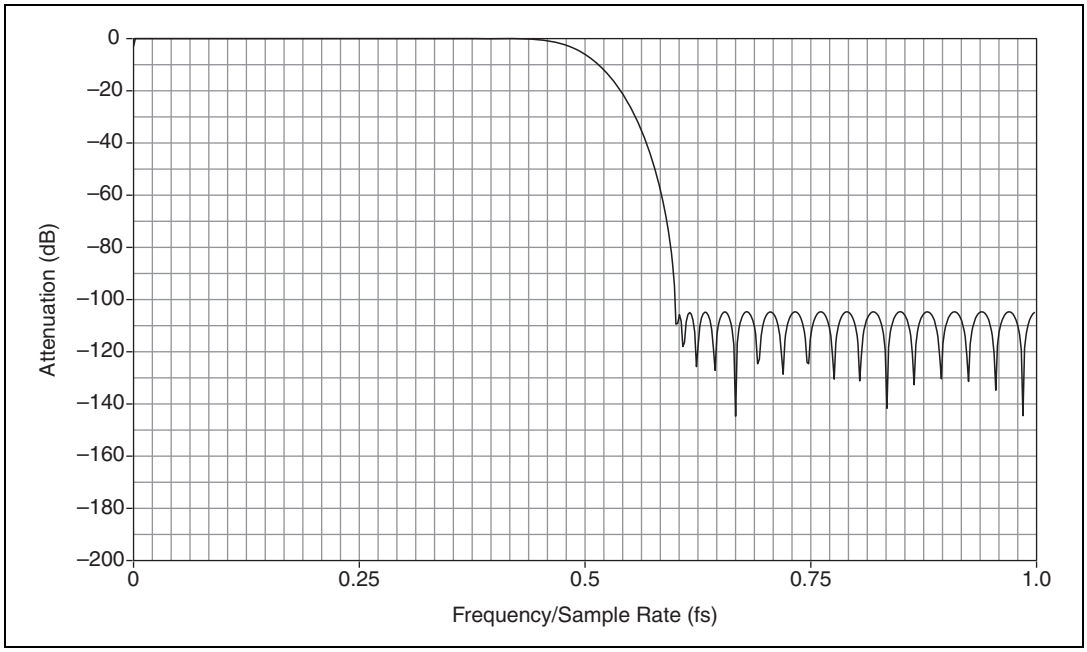

Figure A-37. NI 449*x* Digital Filter Input Frequency Response with Low-Frequency Alias Rejection Enabled

Figure A-38 shows the digital filter input frequency response with low-frequency alias rejection disabled.

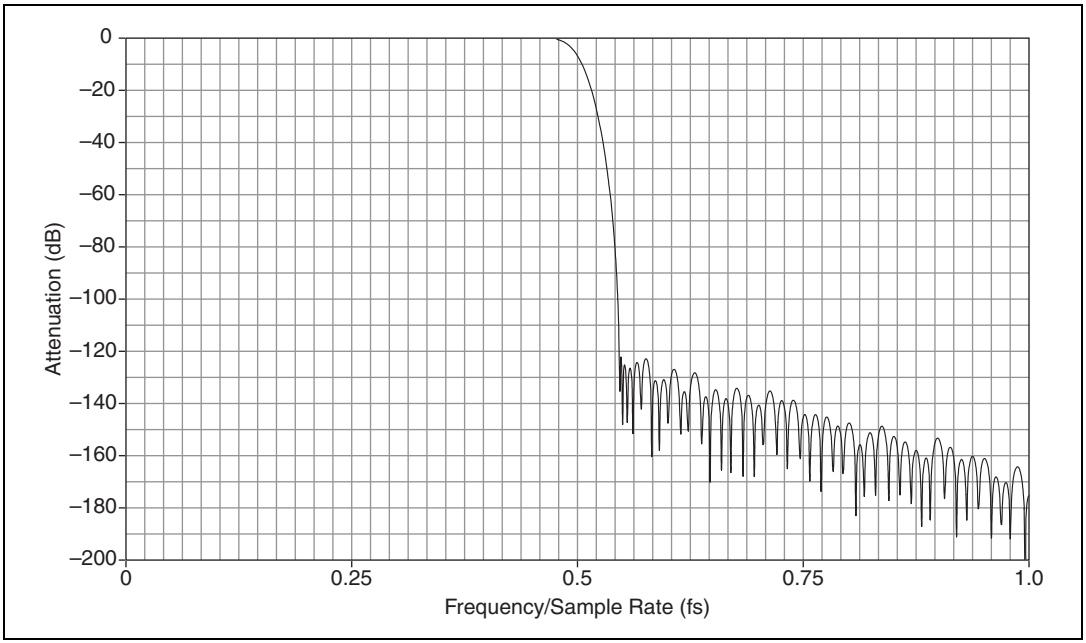

Figure A-38. NI 449*x* Digital Filter Input Frequency Response with Low-Frequency Alias Rejection Disabled

Refer to *Analog Output Filters* in Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about the implementation and functionality of the analog and digital anti-aliasing filters.

Figure A-39 shows the response of the analog anti-aliasing filter with and without enhanced low-frequency alias rejection enabled. Figure A-39 illustrates the alias rejection for a tone that passes the digital filter by falling into one of the f_s-wide bands centered on the oversample rate. The first set of x-axis labels denotes the NI 449*x* sample rate in kS/s. The second set of x-axis labels shows the frequency of an input signal that could pass through the digital filter at the given sampling rate. Refer to the *Anti-Alias Filters* section in Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for information about NI DSA oversample rates. Refer to the *ADC Modulator Oversample Rate* section in the *NI 449x Specifications* for more information.

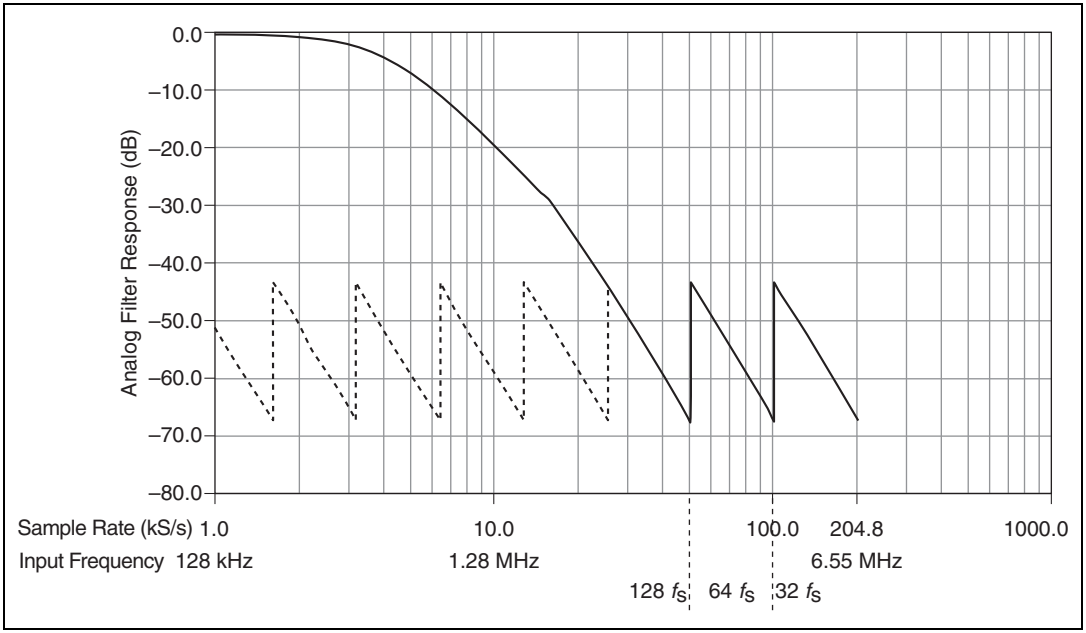

Figure A-39. NI 449*x* Analog Filter Response

For example, when sampling at 10 kS/s, the digital filter will remove any out-of-bandwidth tones up to a 10 kHz band centered on 128 f_s, or 1.28 MHz ±5 kHz. If noise in the input signal falls into this narrow window, the noise is not rejected by the digital filter. In this limited frequency range, you must consider the analog filter. Figure A-39 illustrates that with a sampling rate of 10 kS/s, the analog filter attenuates an input signal frequency of 1.28 MHz by –20 dB without enhanced low frequency alias rejection enabled. With enhanced low frequency alias rejection enabled, the attenuation would be –59 dB.

The sawtooth line in Figure A-39 represents the filter response with low-frequency alias rejection enabled. The worst case alias rejection is approximately –44 dB. This corresponds to the analog filter attenuation at 25.6 kS/s.

This situation represents the worst-case alias rejections for each sampling rate. You would only observe this worst-case scenario with a well-defined tone in a narrow frequency range. In real measurement situations, it is more likely that any energy passing the digital filter consists only of low-amplitude noise. If an unwanted component does appear in the digitized signal, increasing the sampling rate might provide an easy solution by both improving the rejection from the analog filter and by repositioning the digital filter so that it can eliminate the alias.

NI 449*x* Reference Clock Synchronization

NI 449*x* devices employ onboard PLL circuitry. The PLL circuitry locks the onboard 100 MHz voltage-controlled crystal oscillator (VCXO) to the PXI/PXIe 10 MHz reference clock signal, PXI_CLK10. The VCXO output provides the source for the DDS chip, which generates the sample clock timebase. In this way the NI 449*x* devices lock the sample clock timebase to PXI_CLK10.

NI 449*x* Specifications

Refer to the *NI 449x Specifications* for more detailed information about the NI 449*x* devices.

NI 9233 and NI 9234 Devices

Refer to `ni.com/manuals` for documentation about the NI 9233 and NI 9234 devices.

B

Technical Support and Professional Services

Visit the following sections of the award-winning National Instruments Web site at ni.com for technical support and professional services:

- **Support**—Technical support at ni.com/support includes the following resources:
  - **Self-Help Technical Resources**—For answers and solutions, visit ni.com/support for software drivers and updates, a searchable KnowledgeBase, product manuals, step-by-step troubleshooting wizards, thousands of example programs, tutorials, application notes, instrument drivers, and so on. Registered users also receive access to the NI Discussion Forums at ni.com/forums. NI Applications Engineers make sure every question submitted online receives an answer.
  - **Standard Service Program Membership**—This program entitles members to direct access to NI Applications Engineers via phone and email for one-to-one technical support as well as exclusive access to on demand training modules via the Services Resource Center. NI offers complementary membership for a full year after purchase, after which you may renew to continue your benefits.

    For information about other technical support options in your area, visit ni.com/services, or contact your local office at ni.com/contact.
- **Training and Certification**—Visit ni.com/training for self-paced training, eLearning virtual classrooms, interactive CDs, and Certification program information. You also can register for instructor-led, hands-on courses at locations around the world.
- **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, National Instruments Alliance Partner members can help. To learn more, call your local NI office or visit ni.com/alliance.
- **Declaration of Conformity (DoC)**—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting ni.com/certification.
- **Calibration Certificate**—If your product supports calibration, you can obtain the calibration certificate for your product at ni.com/calibration.

If you searched ni.com and could not find the answers you need, contact your local office or NI corporate headquarters. Phone numbers for our worldwide offices are listed at the front of this manual. You also can visit the Worldwide Offices section of ni.com/niglobal to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.